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APPLICATION-SPECIFIC INTEGRATED-MICROELECTROMECHANICAL SYSTEMS (MEMS) PROCESS SERVICES (ASIMPS)

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13. ABSTRACT *(Maximum 200 Words)*
The primary goal of this project was to develop the technology for an application-specific integrated microelectromechanical systems (MEMS) process service, called ASIMPS. Multiple government, industry and academic institutions participated in seven integrated MEMS process runs. Layout rules, design practices and tutorials for integrated MEMS were generated. Microelectromechanical structures were made from the interconnect layers within commercial foundry integrated circuit processes. The post-foundry micromachining process comprised dry etching of the dielectric layers, then a deep-reactive-ion etch of silicon followed by an isotropic silicon undercut to release the structures. An alternate fabrication flow was explored that created single-crystal silicon structures within the foundry processes. Microdevices included accelerometers, gyroscopes, vibratory magnetometers, microphones, microspeakers, scanning mirrors, high quality factor inductors, and tunable capacitors. In particular, microaccelerometers were developed with resolution limited by brownian noise. Millimeter-sized mirrors in the single-crystal silicon process were developed for laser scanning applications. Microspeakers and microphone designs that exploit a unique mesh membrane sealed with polymer were successfully transferred to industry.

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1. Summary

ASIMPS, which stands for Application-Specific Integrated Microelectromechanical systems (MEMS) Process Service, was a project that integrated foundry electronics with MEMS and made the process available to the DoD and MEMS communities. Microelectromechanical structures were made from the interconnect layers within commercial Complementary Metal-Oxide-Semiconductor (CMOS) foundry integrated circuit processes. The use of such foundry electronics processes reduced the cost, risk and time for fabricating custom integrated MEMS for potential military and commercial applications. The post-foundry micromachining process started with a reactive-ion etch (RIE) of the top dielectric layers (mostly silicon oxide and silicon nitride) to define the sidewalls of the micromechanical structures. The structures were subsequently released by etching the silicon substrate to undercut the structures. The silicon etch was performed first with a timed deep-reactive-ion etch to set the spacing between the structures and the substrate. This step was followed by a timed isotropic silicon etch that undercut the structures. The microstructures were, in cross-section, made of stacks of alternating aluminum and silicon oxide layers.

Integrated microstructures with electronics were made starting with 0.6 μm CMOS and 0.35 μm CMOS and Bipolar/CMOS (BiCMOS) processes followed by the post-CMOS micromachining steps. Micromachining was also successful in a CMOS process with copper interconnect and low dielectric constant (low k) silicon oxide instead of aluminum and conventional silicon oxide. A modification to the process flow was explored that created bulk silicon microstructures. In this version of the process, CMOS chips were masked to be exposed in prescribed MEMS regions and then etched from the back-side to thin the silicon to between 25 μm to 60 μm. The chips were then flipped over and the regular post-CMOS micromachining steps were performed. The result was MEMS structures that mixed large bulk silicon structures with microstructures formed from the dielectric and metal layers. Another modification to the base post-CMOS micromachining process was explored to seal large membranes with polymer. After the regular micromachining steps, the devices were exposed to a plasma polymer deposition that sealed gaps of 2 μm or smaller.

Design rules for ASIMPS were identified and values were determined through experimentation. Minimum beam widths were set by the metal interconnect design rules of the foundry and were made down to 0.6 μm. Lateral air gaps between structures were made down to 0.9 μm, though the user design rules were kept at 1.8 μm to relax the processing effort required to open smaller gaps. Microstructures could be made with different thicknesses by designing the top layer to be one of metal 1, 2, 3 or 4 (assuming four metal layers for interconnect in the CMOS process). In many cases, design of beams and plates would benefit from inclusion of the “active” mask, which removed the highly compressive field oxide from underneath the structures. Released structures made with this active mask had less out-of-plane curl. Polysilicon could be incorporated within structures to act as heater resistors or piezoresistors. The timing of the silicon isotropic etch set the maximum width of beams and plates that were guaranteed to be released. Values for this maximum width was dependent on the size of the surrounding gaps formed by slots around beams and holes in the plates. For example, the maximum beam width was 20 μm if 10 μm or larger slots were placed around the beam. The silicon release etch also set the minimum distance of electronics (i.e., transistors and diodes) from a MEMS etch pit that guaranteed their

existence after the micromachining steps. This value was set to 30 μm. The overlap (cut-in) of adjacent metal to metal layers to form microstructures was constrained to at least 0.3 μm to assure a continuous microstructure in the presence of any layer misalignment. The polysilicon layer was required to be enclosed by metal 1 by at least 0.3 μm to assure that it would not be etched during the substrate etch step in the presence of any layer misalignment. The polysilicon layer also required presence of the CMOS field oxide underneath as protection from the silicon etch step.

While refining the ASIMPS process for general uses, several issues specific to the post-foundry CMOS micromachining were identified. Critical dimensions defined by the top metal layer (i.e. metal 4) in the particular 0.35 μm CMOS processes used in the project were affected by linewidth bloat, by offset of the top metal layer with the underlying layers and by excessive polymer deposition on the structural sidewalls. Gaps less than about 1.8 μm between structures were restricted to definition using the lower metal 1, 2, and 3 layers. During the dielectric etch, aluminum from the mask layer incorporated into the plasma and, at critical levels of exposed aluminum area (chip or wafer areas over about 6 mm^2), created excessive polymer sidewall deposition. This phenomenon occurred for all metal layers, and was exacerbated on sidewall edges defined by metal 4. Photoresist masking of the aluminum in the field regions on wafers and large chips solved this problem.

Multiple government, industry and academic institutions participated in seven integrated MEMS process runs during the project. Layout rules, design practices and tutorials for integrated MEMS were generated. Five ASIMPS short courses were held to introduce the process and teach design principles. Custom ASIMPS design kits built upon commercial design environments from Cadence and Tanner MEMSPro were created and supported by MEMSCAP. The design kits included MEMS design rule checks, MEMS all-angle layout, basic layout generators, 2-D cross-section viewing from layout, and 3-D solid model generation from layout for import to finite element analysis. The Carnegie Mellon Nodal Analysis of Sensors and Actuators (NODAS) model library for MEMS design was expanded to include improved linear beam and plate models, non-linear beam and plate models and electrostatic gap models. The models supported the multi-layer CMOS MEMS structures with multiple structure thicknesses and electrical wiring capability. An extraction algorithm for CMOS MEMS was refined to assist in verification of layout vs. schematic. Parasitic extraction of capacitances in MEMS regions was also supported.

Microdevices made within the ASIMPS included accelerometers, gyroscopes, vibratory magnetometers, microphones, microspeakers, scanning mirrors, high-quality factor inductors, and tunable capacitors. At Carnegie Mellon, microaccelerometers were developed with resolution limited by brownian noise. An initial prototype of high-g accelerometer arrays were created. Millimeter-sized mirrors in the single-crystal silicon process were developed for endoscopic optical coherence tomography. The 1 mm^2 mirrors were adequately flat and large to allow scanning of laser beams with widths up to several 100 microns. Electrothermal actuation provided scanning range up to 45°. Microspeakers and microphone designs that exploit a unique mesh membrane sealed with polymer were successfully transferred to Akustica, Inc. for commercialization. The ASIMPS research demonstrated the feasibility of achieving low noise microphones and audible in-ear speakers with the technology.

2. Introduction

The goal of this project was to develop design, fabrication and characterization support for monolithically integrated systems merging sensing and actuation with computing and communication. Single-chip integration of these various functions was enabled via a CMOS micromachining process offered as a user service and with computer-aided design tools to enable the design and implementation of low cost and low volume application-specific integrated MEMS. (CMOS stands for "Complementary Metal-Oxide Semiconductor" electronics and is the predominant foundry process used to make almost all digital electronics.) Additional goals of this project were to make CMOS micromachining accessible for prototyping and manufacturing, and to demonstrate the versatility of the CMOS MEMS process through development of a variety of microdevices.

Devices designed and fabricated in the resulting foundry process included accelerometers, gyroscopes, radio frequency (RF) MEMS communication systems (with resonator oscillators, RF filters and high-Q inductors), infrared sensors and imagers, acoustic transducers, electrothermal converters, and force sensors.

In 1993, DARPA funded the initial work on a polysilicon Multi-User MEMS Process Service called MUMPs and run by MCNC [1]. The MEMS unit within MCNC was spun off into a company called Cronos Integrated Microsystems. JDS Uniphase acquired Cronos and subsequently sold the division to MEMSCAP. Single-crystal silicon and metal MUMPs processes were created by MEMSCAP as a natural extension of the polysilicon surface micromachined offering. Throughout this time, MUMPs has flourished, with commercial and DoD users inventing new applications and devices which were not foreseen when the service was first offered. ASIMPS was created in an effort to jump-start a process service where MEMS would be directly integrated on-chip with electronics. Carnegie Mellon had expertise in making CMOS MEMS and Cronos/MEMSCAP had expertise in commercialization of MEMS process services, and so a natural project team was formed.

An exciting and essential feature of ASIMPS is inclusion of various multiple devices on the same chip with supporting electronics. The vision is to have the integrated MEMS process available for prototyping so system and circuit designers can invent new microsystems with levels of complexity previously unachievable by the MEMS community alone. For example, high-Q inductors and resonators can be combined with CMOS RF electronics to form voltage controlled oscillators, low-noise amplifiers, filters and mixers. In another example, multiple accelerometers can be integrated on chip to create customized inertial measurement systems. For example, low-g accelerometers that overrange can be made to pass off sensing responsibility to very high-g accelerometers. To further the impact, both the communications and accelerometer systems can be combined to form wireless microsensor system. Such a system is primarily driven by low-volume applications and will not be commercially viable if manufactured in specialized MEMS processes. Realization of these kinds of systems is within reach of the CMOS micromachining technology and through ASIMPS, reduces to a problem of design effort and end-application know-how, not of process development.

3. Methods, Assumptions, and Procedures

The general organization of the ASIMPS project is summarized in Figure 1. The project was divided into three main tasks: CMOS-MEMS Manufacturing and Process Development, Design Support and Development, and the Alpha User and Technology Driver. Users of the process service designed integrated MEMS designs using computer aided tools supplied by the design support task. Layout from various users on a given run were tiled into a master layout and sent to a CMOS foundry. The CMOS wafers, or in some cases chips, were then subjected to the post-CMOS micromachining

The initial manufacturing plan was to have Cronos Integrated Microsystems, Inc. support the post-CMOS process and perform packaging. However, shortly after the project started, Cronos was purchased by JDS Uniphase, which changed their relationship in the project. Carnegie Mellon then assumed the role of performing the fabrication for beta users of the process service. MEMSCAP provided design support, and Carnegie Mellon acted as the technology driver for CMOS-based MEMS development and assumed overall project management.

The post-CMOS micromachining process that was used in ASIMPS is detailed in Figure 2. The micromachining process started with conventional foundry CMOS. A dry CHF_3:O_2 dielectric etch defined the structural sidewalls. Then a dry SF_6 (or XeF_2) etch removed silicon under the structures for release. In prior work at Carnegie Mellon, micromechanical devices post-processed from four processes available from MOSIS (Hewlett-Packard (HP) 0.8 µm, 0.5 µm, 0.35 µm CMOS, and TSMC 0.35 µm CMOS) were successfully fabricated and electromechanically tested. Prior to the project, micromechanical material properties were characterized in the HP 0.5 µm process. A milli-g lateral capacitive accelerometer was successfully fabricated and tested.

ASIMPS used CMOS direct from a foundry to minimize costs and to have access to full wafers. Cronos reached an agreement with the Austria Mikro Systeme (AMS) foundry to perform the base CMOS process. The initial post-CMOS process started with recipes developed at Carnegie Mellon for MEMS made with the HP 0.5 µm CMOS process. Measurements on process and device characterization structures were performed to determine the best processing conditions for the AMS CMOS process chosen.

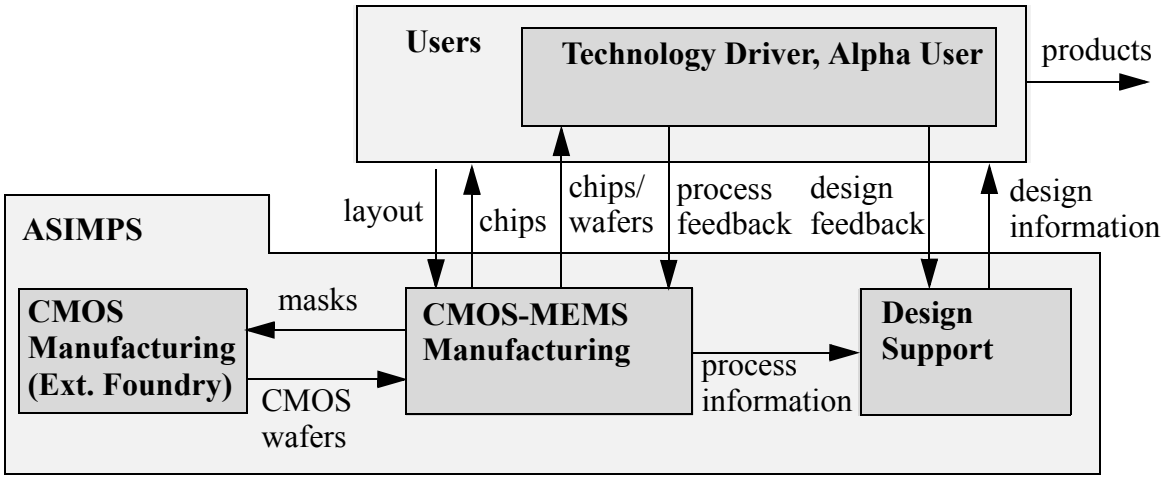


FIGURE 1. Application-Specific Integrated MEMS Process Service (ASIMPS).

The formation of microstructures were performed in three different manners: either through use of a metal layer as an etch mask, or with the addition of an aligned photoresist layer after CMOS is completed, or with a separately defined metal mask after CMOS is completed (Figure 2). The trade-offs between the methods are as follows:

- Method #1: Use of a CMOS metal layer as the structural etch mask provided a self-aligned, minimum feature process. This eliminated the need for additional lithographic processing, and improved throughput time. The dielectric etch with an aluminum mask had been demonstrated to provide high-aspect-ratio sidewalls necessary for narrow gaps and narrow beam widths. However, in order to minimize damage to the metal layer from sputtering (i.e. ion milling) during etching, which can also contaminate the wafer and process chamber, the process was required to be run at low power. This increased the etch time and negatively impacted yield and cost.
- Method #2: To eliminate the sputtering damage in method #1, the wafers or chips could be processed with an exposed photoresist layer to produce the etch mask. This would protect the CMOS metal layers during the etch process. However, this requires alignment of the mask to the underlying metal layers, which introduces misalignment between the etch mask and the metal. This approach would require larger feature sizes (a few tenths-of-microns) to accommodate this misalignment. An adequate process would need to be developed to ensure high-aspect-ratio dielectric sidewalls with the photoresist mask. The process must operate at high enough etch power for reasonable etch times, and require thick resist.
- Method #3: A separate patterned metal mask could protect the CMOS metal layers, but would have the same alignment issues as method #2. The metal could be tailored to allow a high-power etch giving potentially a high yield and low cost. However the added complexity of introducing a new metal sputtering and patterning process on top of the CMOS could offset the gain in yield during the structural etch.

Test structures for process and device characterization were compiled by modifying existing test structures for the HP process. Some test structures were already developed at Carnegie Mellon, including beam resonator arrays for elastic modulus, fatigue resonators for stress fracture, perforated plates and substrate resistors for undercut, clamped beam arrays for residual stress, and composite beam arrays for lateral and vertical stress gradients and for mechanical effects from

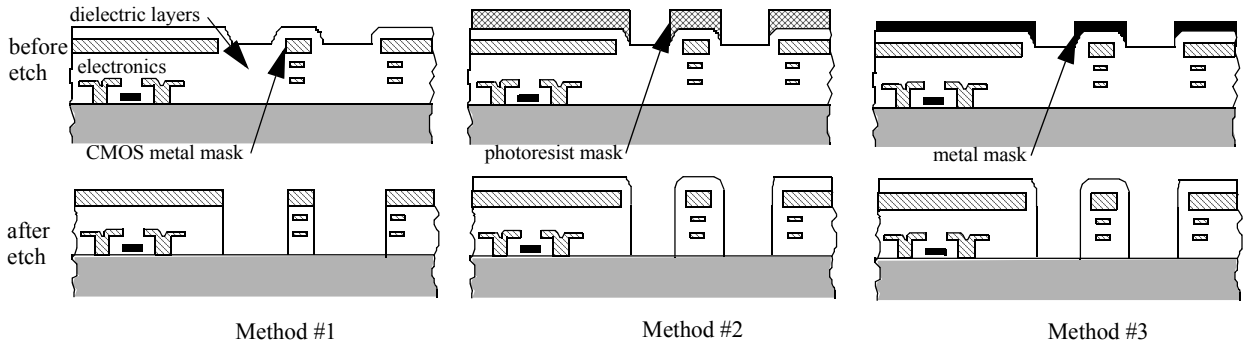


FIGURE 2. Methods for masking the dielectric to form the microstructural sidewalls in CMOS. Method #1: Self-aligned CMOS metal mask. Method #2: Post-CMOS photoresist mask. Method #3: Post-CMOS metal mask.

internal layer offsets. These layouts provided a good starting point for development of ASIMPS test structures. Information from test structures on the ASIMPS runs were used iteratively to improve the manufacturability of the post-CMOS dry etch process steps, and to generate and verify design rules.

While establishing the MUMPs process in 1993, it was learned that the involvement of 'expert external users' greatly aids the refinement of the multi-user process. The variability of design style, the use of non-intuitive (to the process designer) rule combinations and the influx of new ideas helped to 'break' and 'remake' that process. The ASIMPS project used this same method to help develop, establish and stabilize the process before full-scale rollout to the user community. A number of external users developed test structures, devices and 'systems' that were run along side the project teams designs. This beta-user activity helped to make the process robust enough to prove feasibility to make the process service available to a wider user community.

ASIMPS process was developed with test runs for the internal project members and separate alpha user runs for groups with some prior MEMS design experience. The test runs were restricted to process and design development. The alpha runs ramped up from two offerings in 2001, one each in 2002 and 2003, and four in 2004. The ASIMPS design kits were developed by MEMScAP in parallel with the initial process offerings and were gradually populated with the rules, cells, primitives and elements necessary to aid the user in quick and successful development of their projects, with response to feedback from the alpha users. It was expected at the beginning of the project that Cronos would be responsible for the interface service (order and data collection, foundry interface, post-processing and packaging). However, their purchase by JDS Uniphase required a shift in that responsibility to MEMScAP and Carnegie Mellon. Upon purchase of the MEMS division from JDS Uniphase, MEMScAP revived the potential for commercialization of ASIMPS by their company.

The core of activity in the Design Support Task involved customization through model development of the MEMScAP MEMS Engineering Kit. The Engineering Kit, shown in Figure 3, is a design framework that combines aspects of electronic design automation with mechanical, thermal, and fluidic computer-aided design. The Kit initially supported MUMPs along with a few other process flows from MEMS foundries. The effort in this task was to generate the necessary modeling information to customize the existing environment for ASIMPS. The core software incorporates the Cadence design environment as a standard design option and the Tanner MEMSPro environment as a lower cost option. The environment contains elements for the device designer, enabling design, simulation and the ability to form characterized standard cells in a library. Commercially available optimization and yield management tools, such as OPSIM and ASPIRE were extended to MEMS technology to enhance the work of the MEMS device engineers. The MEMS Engineering Kit supporting this technology was made available to universities and selected groups at significantly reduced rates in order to facilitate initial use of ASIMPS and build a base of experienced users.

Functional simulation of microelectromechanical systems (MEMS) and microcomponents is a critical part of efficient integrated MEMS design. Such simulation can be done efficiently by using a single system description language suitable for a single mixed-mode simulator. The advent of analog Hardware Description Languages (AHDLs) such as HDL-A by Mentor Graphics, Verilog-A by Cadence, and the future standard VHDL-AMS enabled creation of behavioral

models of electrical and non-electrical devices. Carnegie Mellon's NODAS (Nodal Design of Actuators and Sensors) was initiated with prior DARPA funding to form a hierarchical circuit representation of MEMS implemented as a design library of interoperable building-block MEMS elements. Schematic symbols and models for 2D polysilicon beams, plates, gaps, and anchors were connected together to represent any suspended MEMS device. In ASIMPS, these models were expanded to include multiple conductors in the CMOS microstructures, which alter the mechanics, capacitance, and electrostatic force. 3D models for multiple-conductor beams, plates and gaps were added to support design of ASIMPS microstructures. Vertical curl from stress gradients in the composite structures is very important in design, so mechanisms for predicting curl within the NODAS schematic were investigated.

In the Alpha-User Task, a design effort to create high-shock accelerometers directly in ASIMPS was undertaken. Accelerometer design for high shock and vibration built on research at Carnegie Mellon on low-g inertial sensors. Prior to this effort, a CMOS-MEMS lateral capacitive accelerometer topology, inspired by the Analog Devices line of accelerometers, was designed and fabricated and one prototype was successfully tested. Accelerometers that must withstand over 40,000 G have significantly different design constraints from low-g devices. The design approach taken in this project was to develop a simple, stiff accelerometer with a small proof mass to achieve sufficiently high resonance frequency and low sensitivity to measure greater than 10,000 g accelerations without saturating, and then array many of these accelerometers in parallel to raise the sensitivity for superior signal to noise performance.

Another Alpha-User thrust extended ASIMPS to a new application domain, acoustic MEMS, that is different from prior applications in CMOS micromachining. The first device to be investigated was an integrated micromachined acoustic (and audible) speaker that fits completely inside the ear canal (16 mm^2 chip). The MEMS earphone and ear canal formed a sealed, closed cavity where the acoustic wavelengths were greater than the size of the ear canal (~ 2 cm) for most of the frequencies of interest (frequencies within the range of human hearing). The acoustic devices were made by first creating a fine metal mesh using the post-CMOS micromachining process. An additional polymer deposition processing step was then employed to seal the mesh to form an air

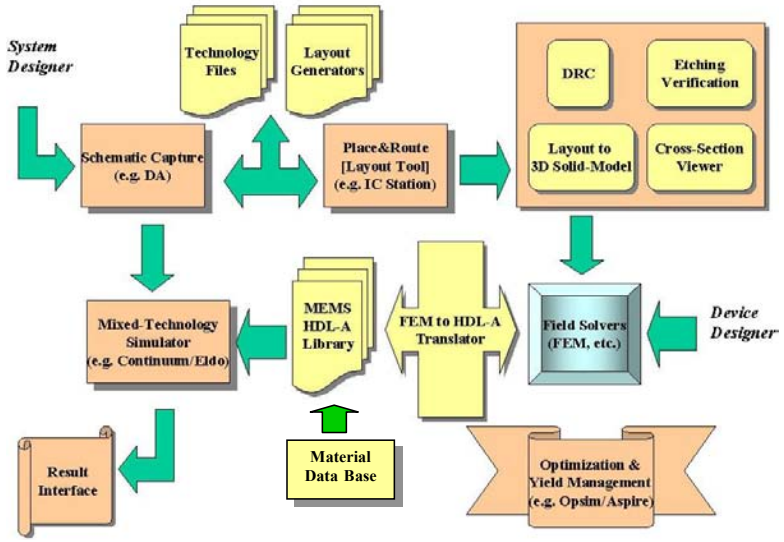


FIGURE 3. MEMSCAP MEMS Engineering Kit environment.

tight membrane. Calculations showed that a 4 mm^2 membrane with a peak deflection of 1 µm and a 2 cm × 1 cm × 1 cm ear canal, the pressure level at the eardrum is approximately 83 dB SPL (sound pressure level), well above the 45-65 dB SPL hearing thresholds for human adults with normal hearing. The integrated micromachined speakers enabled novel acoustic MEMS speaker architecture explorations including pulse-width modulated, two-state acoustic membrane speakers (with inherent, mechanical digital-to-analog conversion) and a distributed-array speaker implementation employing numerous digital speakers or "speaklets", which collectively produce the desired acoustic waveforms. The speaker technology also enabled development of microphones, which were then spun off commercially by Akustica.

4. Results and Discussion

4.1 ASIMPS CMOS-MEMS Processing

Process History. The post-CMOS micromachining processing prior to the ASIMPS project was developed primarily using the Hewlett-Packard (now Agilent) 0.8 µm and 0.5 µm 3-metal CMOS processes. One goal in ASIMPS was to investigate full wafer processing, which was not available through the HP processes. The ASIMPS development began with use of the Austria Mikro Systems (AMS) 0.6 µm 3-metal CMOS and shifted in late 2002 to use the Jazz Semiconductor 0.35 µm 4-metal SiGe BiCMOS. Both foundries were willing to provide wafers as required for the project development. Table 1 is a summary of the CMOS-MEMS wafer runs during the project. Six AMS design runs and five Jazz design runs were completed during the project.

The first two ASIMPS runs were fabricated in AMS's 100 mm (4" diameter) wafer processing line, because processing equipment at Cronos was limited to handling this wafer size. The 100 mm line was an experimental fabrication line for the AMS 0.6 µm triple-metal double-poly high-resistive poly CMOS process. Unfortunately, the metallization and dielectrics in this particular process turned out to have poor dimensional control, resulting in poor quality micromechanical devices. The resulting released structures showed significant evidence of polymerization and large vertical stress gradients. A focused-ion beam etched (FIBE) cross-section of the metal-dielectric stack prior to micromachining from the 4" wafers received from the first alpha run is shown in Figure 4. The cross-section shows two of the common sub-micron CMOS process features: chem-mechanical polishing

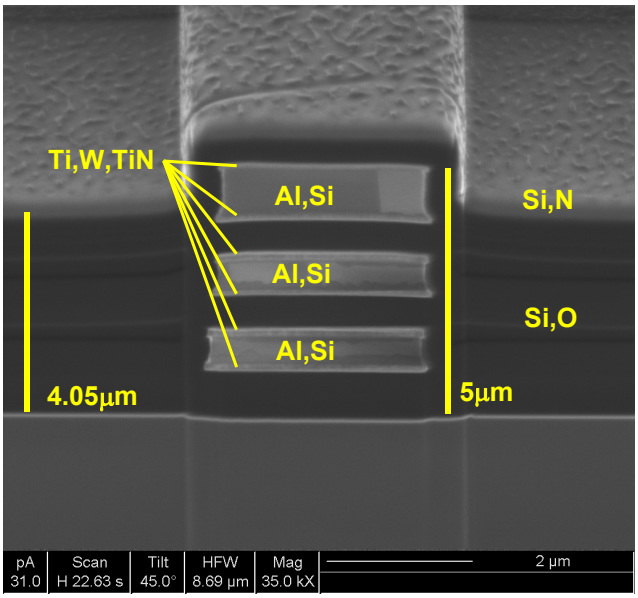


FIGURE 4. FIB cross-section from the first alpha run in the AMS 0.6 µm CMOS, before micromachining steps.

Table 1: Summary of ASIMPS Runs

Run Name	Wafer Size	Short Course	Tape Out	Fab Out	Dice returned	Processing
Test #1 (5 wafers)	4”	N/A	August, 1999	Nov., 1999		Die-level processing at CMU
Test #2 (25 wafers)	6” (re-fab of Test Run 1)	N/A	March, 2000	July, 2000		4” wafers returned; used in wafer-level screening experiments
Test #3 (25 wafers)	6” (re-fab of Test Run 2)	N/A	July, 2000	Nov., 2000		6” wafers returned; Held back characterization of improved dielectric etch characterization
Alpha #1 (25 wafers)	6”	July 20-21, 2000	Dec. 15, 2000	April 6, 2001	May, 2001	21, 6” wafers returned; 1 wafer processed at die level and delivered to alpha users; remainder used for improved dielectric characterization
Alpha #2 (10 wafers)	6”	March 26-27, 2001	July 12, 2001	Sept. 4, 2001	Oct., 2001	10, 6” wafers returned; 1 wafer processed at die level and delivered to alpha users; remainder used for verification of wafer-level process
Alpha #3 (10 wafers)	6”	January 10-11, 2002	April 10, 2002	July, 2002	August, 2002	10, 6” wafers returned; 1 wafer processed at die level and delivered to alpha users; remainder used for verification of wafer-level process
Test #4 (Jazz shuttle run)	5 mm by 5 mm	N/A	Dec., 2002	Feb., 2003	N/A	100, 5 mm by 5 mm chips returned; several chips processed at die level at CMU
Alpha #4 (Jazz shuttle run)	Two 5 mm by 5 mm chips	May 1-2, 2003	July 15, 2003	Oct. 2003	Nov. 2003	100, 5 mm by 5 mm chips of the two submitted chips were made by Jazz; several chips processed at die level at CMU.
Alpha #5 (Jazz shuttle run)	Two 5 mm by 5 mm chips	N/A	November 17, 2003	February 25, 2004	Apr. 2004	100, 5 mm by 5 mm chips of the two submitted chips were returned; several chips processed at die level at CMU.
Alpha #6 (Jazz shuttle run)	5 mm by 5 mm	N/A	January 20, 2004	May 6, 2004	Jun. 2004	100, 5 mm by 5 mm chips of the two submitted chips were made by Jazz; several chips processed at die level at CMU.
Alpha #7 (Jazz shuttle run)	5 mm by 5 mm	May 2004	May 18, 2004	July 29, 2004	Sept. 2004	100, 5 mm by 5 mm chips of the two submitted chips were returned; several chips processed at die level at CMU.

(CMP) is used prior to metallization in the higher level metal layers, and refractory-metal clad layers (e.g., titanium, titanium nitride, tungsten, or combinations of these materials) are used to aid in the metal-oxide adhesion. The fluorine based etchants used in the silicon oxide sidewall etch step and in the silicon release step also etch titanium and tungsten. This concern led to use of a mixture of CHF_3 and O_2 during the dielectric etch, with process operation at a point where a small amount of polymerization occurs on sidewalls, as was done in previous post-CMOS micromachining processing. The thin polymer layer over the dielectric sidewalls protects the refractory metal layers from attack.

The third test run and the subsequent first three alpha-user runs utilized the AMS 150 mm (6" diameter) 3-metal 0.6 μm CMOS process, made by XFab in Germany. The process provided better sidewall geometry control for the microstructures than the 100 mm wafer process. However, the vertical curl for residual stress gradients remained large. In late 2002, a switch was made to the California-based Jazz 4-metal 0.35 μm SiGe BiCMOS process on 8" wafers. An arrangement was made to use Jazz' multi-user prototyping service through an agreement with MEMSCAP (who purchased JDS Uniphase's MEMS division, formerly Cronos). Four Jazz CMOS-MEMS alpha-user design runs were taped out between 2002 and the close of the project in June 2004. Micromachining using the Jazz BiCMOS process yielded very flat microstructures.

Dielectric RIE for CMOS-MEMS Sidewalls. The dielectric etch process for ASIMPS was developed at Carnegie Mellon on individual CMOS die in a PlasmaTherm 790 reactive-ion etch (RIE) system with a 6" carbon platen. The complete post-CMOS micromachining process details are documented in a Ph.D. thesis [2]. JDS Uniphase, who purchased Cronos, was using a PlasmaTherm 740 RIE with an 11" aluminum platen for their dielectric etch screening experiments. To develop the process in house, JDS Uniphase created a set of "mock CMOS" wafers with a 4 to 5 μm-thick phosphosilicate glass layer with a top aluminum mask layer. These layers were meant to approximate the back-end layer stack in a foundry CMOS process. The dielectric etching of "mock CMOS" wafers performed at JDS Uniphase resulted in incomplete etch through the dielectric. A roughened wafer surface was observed in regions where the aluminum did not mask the dielectric. Initially, this was believed to be an etching artifact of the difference between the foundry and mock CMOS wafer dielectric and metal materials. However, screening experiments using the foundry CMOS wafers showed the same roughened surface in areas where there was narrow openings in the aluminum mask, and an incomplete dielectric etch in areas with wide aluminum mask openings. Furthermore, etch depth variation ranged from 3% on one location on the wafer to 16% on a different location in the wafer.

A whole-wafer etch of the foundry CMOS wafer using the optimized die-level process was then performed at Carnegie Mellon, with similar results to the JDS Uniphase experiment. Investigation of the wafer indicated that there was no difference between etching large die or wafers at 60 min into the etch. The areas meant to be opened for subsequent silicon release etching turned black by 120 min into the etch process, as seen in the microscope photos of Figure 5(a) and (b). The blackened area is shown in Figure 5(c) and (d). The area is completely covered with 0.1 to 0.3 μm wide pillars having 0.1 to 0.3 μm spacing in a random pattern. Analysis showed that the pillars contain Si, Al, F, O, and Ti while the areas between pillars contain Si, O and F. Furthermore, as shown in Figure 6, Al and F appeared with Si on the beam sidewalls. This data suggests

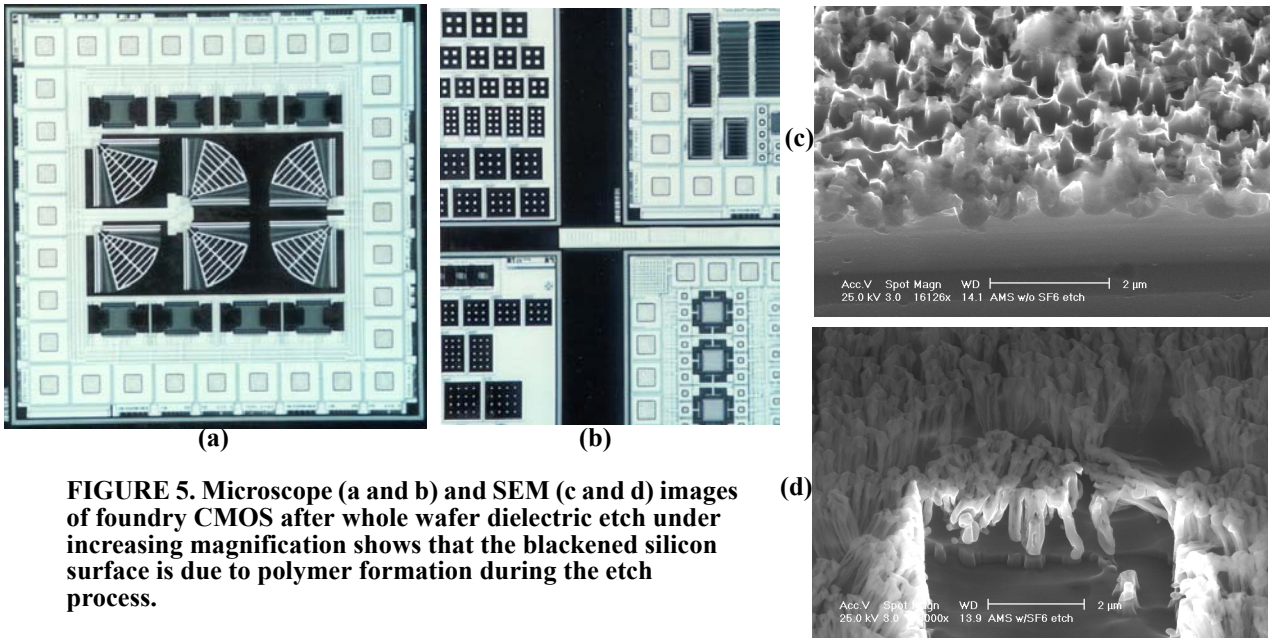


FIGURE 5. Microscope (a and b) and SEM (c and d) images of foundry CMOS after whole wafer dielectric etch under increasing magnification shows that the blackened silicon surface is due to polymer formation during the etch process.

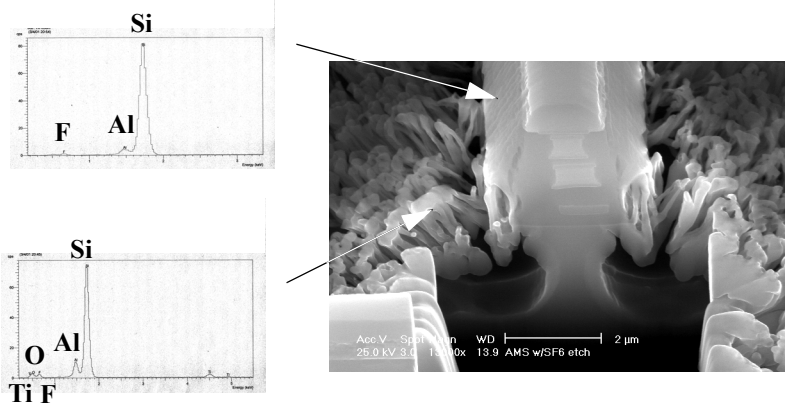
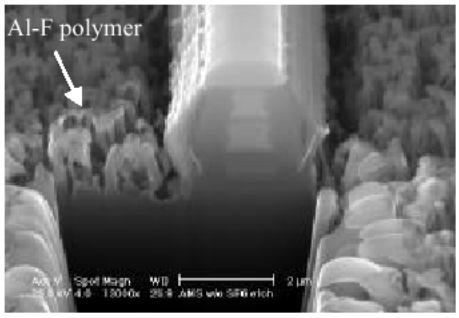


FIGURE 6. Analysis results of the polymer on beam sidewall and Si field shows Si, Al, F, O, and Ti on the stalagmite and Si, Al and F on the beam sidewall

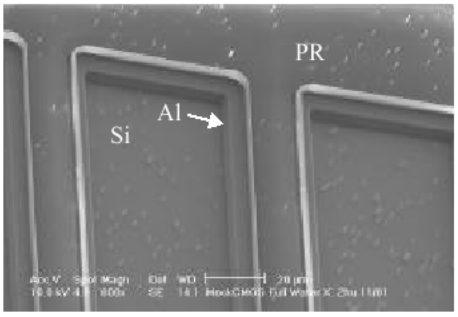
that the aluminum mask was re-sputtering onto the field and creating polymers with aluminum content.

The polymerization during the dielectric etch was dependent on the amount of aluminum exposed to the RIE ion impingement. Die-level processing in the reactor with the carbon platen did not experience this problem. Many smaller dice, spread evenly across the platen also did not experience problems during dielectric etch. However, when using the same reactor with an aluminum platen, die-level processing for any die size experienced the polymerization.

The best method of solving the dielectric etch problem is to make a contact mask that covers the "non-MEMS" areas on the wafer that are covered with aluminum. This aluminum protection mask may be formed by bloating the logical combination of all metal layers by 10 µm, then shrinking by 20 µm. Therefore, all structures less than 20 µm wide are unprotected by the photoresist mask. It requires crude (10 µm) alignment and relatively large feature sizes. The mask blocks a majority of the aluminum on the wafer during the oxide etch step. The aluminum layers

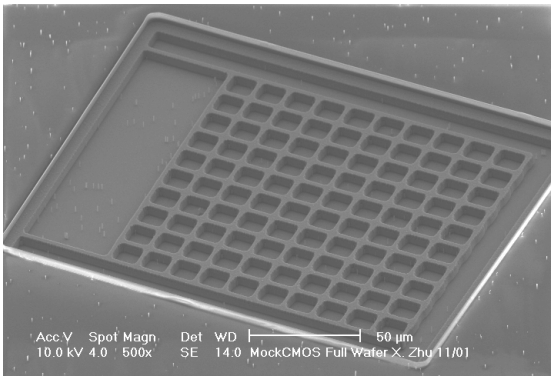


(a)

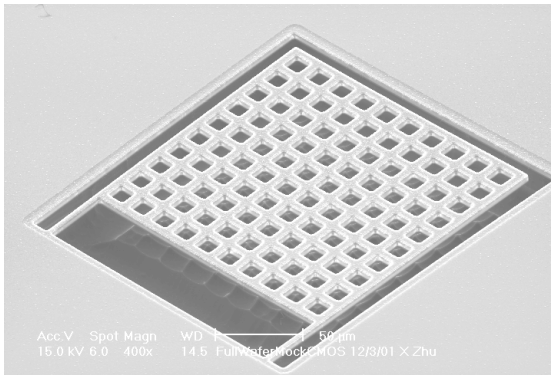


(b)

FIGURE 7. The microstructural SiO_2 etch at the wafer scale. (a) Without the photoresist aluminum-protection mask, the field is covered with a thick layer of Al-F polymer, inhibiting the etch. (b) With the photoresist mask, obtained by shrinking the original aluminum structural mask by 5 μm, the etch does not exhibit polymerization.



(a)



(b)

FIGURE 8. (a) Mock-CMOS wafer after dielectric RIE. No problems are evident since past polymerization problem is resolved. The rim from the photoresist protection mask surrounding the test device is evident. (b) A microstructure after silicon DRIE release. The substrate in the etch-pit area is smooth and the microstructure surface is clean.

near the edge of the etch pits remain exposed, so that the critical dimensions of microstructural beam widths and gaps remain set by the metal layers (i.e. by the fine-line CMOS interconnect design rules). The ability to make multi-thickness structures also remains intact. As an example, for the alpha-1 run, out of the total reticle area of 400 mm^2, the aluminum in the MEMS area was 39 mm^2 and aluminum in the non-MEMS area covered by the aluminum protection mask was 203 mm^2.

The aluminum protection mask increased the wafer-level dielectric etch rate by 54% by eliminating the source of the excess polymerization. The comparison of dielectric etch with and without the photoresist protection mask is shown in Figure 7 on a mock-CMOS wafer. The wafer-scale SiO_2 etch rate was only reduced by 20% compared to the etch rate on individual dice. No micromasking effect was observed in the release step of the Si etch, as seen in Figure 8.

Based on current equipment parameter settings, the dielectric etch rates on a set of trenches

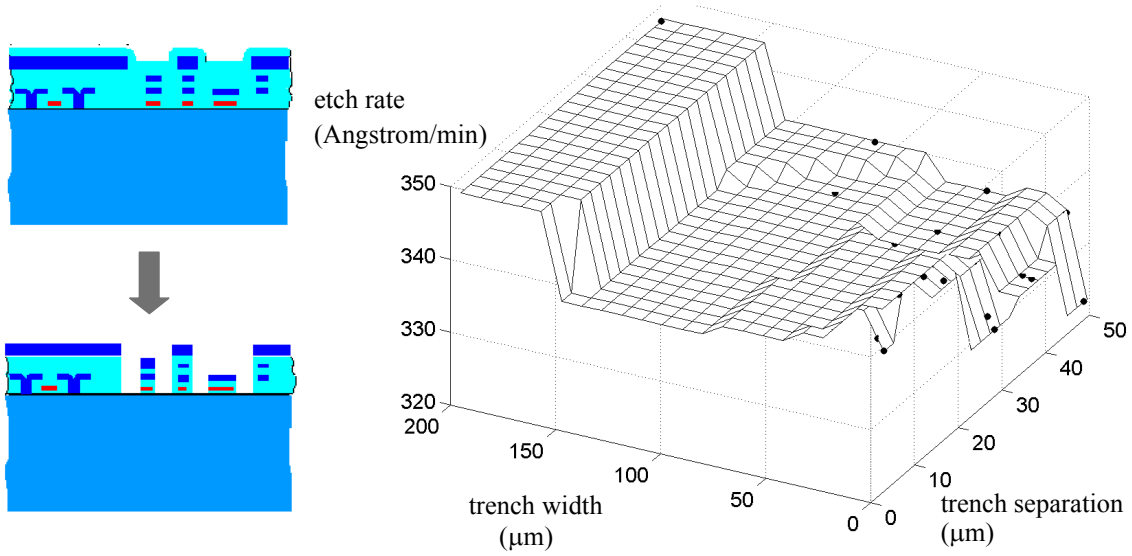


FIGURE 9. Etch lag of RIE oxide on different test trench patterns with an 100 min etch and O_2 flow at 16 sccm.

with different combination of trench width and trench spacing were measured. The experiment was done with a process condition of 125 mTorr pressure, 0.55 W/cm^2 power, 22.5 sccm CHF_3 flow and 16 sccm O_2 flow. The etch rate as a function of trench width and trench separation is shown in Figure 9. When the etch does not exceed 2 μm in depth, maximum height to width ratio was about 1:1. In this case, the etch rate variation was not very sensitive to the change of trench width from 2 μm to 100 μm wide, and to the density of trench placement from 2 μm to 50 μm separation. An 100 times increase in trench width caused only a 7.8 % increase in etch rate. Increase in trench spacing did not have an obvious affect on etch rate.

The physical bombardment is the key characteristic in this etch. As illustrated in Figure 10, the direction of incident ions are not perpendicular to the etched surface, it has a distributions with incident angles. Unless the height to width aspect ratio is greatly over 1:1, which limits the number of ions that reach the bottom of trench, there is no difference on etch rate between wide and narrow trenches. And there is no difference between sparse and dense trench arrays. However, when the aspect ratio is greater or equal to 2:1, the size of trench opening limits the number of ions that reach the bottom. It also limits the by-products of reaction being taken out of the trench, and consequently, reduces the concentration of reactive radicals at the surface and reduces the etch rate.

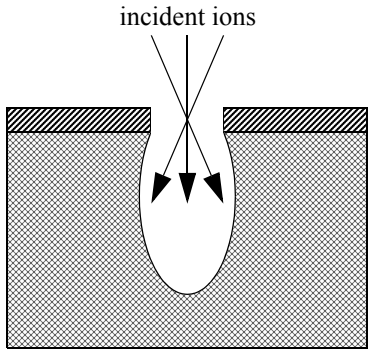


FIGURE 10. Angular distribution of incident ions

As illustrated in Figure 11, a 170 min dielectric etch was conducted on the same test pattern.

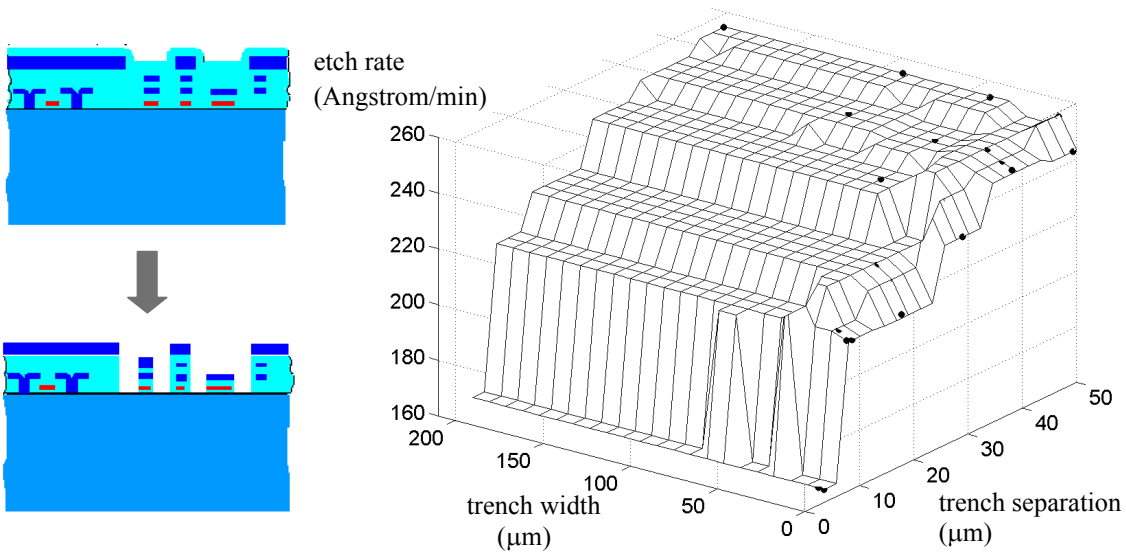


FIGURE 11. Etch lag of RIE oxide on different test trench patterns with an 170 min etch and O_2 flow at 5 sccm. Note the scale is much larger than in the previous figure.

The O_2 flow rate was set at 5.0 sccm in order to use photoresist to cover most of metal area in the etch. The overall etch rate slowed down. The higher aspect-ratio contributed to not only slow the etch rate but also to increase the etch lag. Comparing etch depth on a 2 μm versus 200 μm trench, the etch lag was as high as 40%; but the etch lag was less than 20% between a 6 μm and 200 μm trench, where the height-to-width aspect ratio was less than 1.

To guarantee the complete etch through dielectric layers with different openings, especially when considering comb finger structures with height to width aspect ratio over 2.5, at least 20% overetch is usually conducted. Therefore, a 1.8 μm comb finger spacing design rule (corresponding to 2.8:1 height-aspect-ratio) was dictated for conservative design. A lower spacing value dramatically increased the processing time.

Further characterization of the dielectric etch process was required after migrating to the Jazz BiCMOS process. An initial test wafer contained device and interconnect test structures used by Jazz for qualifying their process. It was diced into 3 mm by 3 mm chips, and post-CMOS micromachined using the ASIMPS post-processing recipe. This dicing was done to emulate the sizes that have been used in the ASIMPS die level processing in the past. Reactive-ion etch (RIE) of 26 of these chips was performed with 32 sccm O_2 flow, 22.5 sccm CHF_3 flow, 125 mT chamber pressure, and 100 W power for about 2 hours to etch the passivation and underlying oxide dielectric layers that define the structural sidewalls. Subsequently, isotropic deep RIE silicon (DRIE) of 12 of these chips followed by an anisotropic silicon etch for final release was performed. Sample scanning electron micrographs (SEMs) are shown in Figure 12. The released structures look similar to those from other CMOS foundry processes. Unlike the AMS 0.6 μm CMOS process, there was no obvious polymer by-products in the gaps. The metal-3 and metal-4 structures displayed much less vertical curl than the AMS 3-metal structures, as illustrated in Figure 12. Structures composed of metal-1 and underlying field oxide are about 1 μm thick and exhibit significant ver-

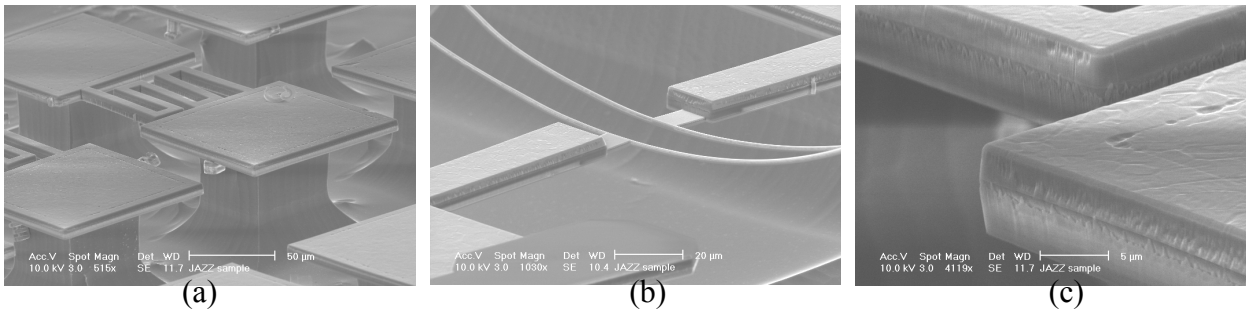


FIGURE 12. SEM micrographs of Jazz semiconductor interconnect test structures.

tical curl as shown in Figure 12(b).

Three primary issues impacting the micromachining were identified while processing the Jazz chips: (a) polymer deposition on sidewalls, (b) structural mask bloat, and (c) excessive metal layer misalignment. The dielectric RIE on chips larger than around 6 mm^2 led to polymerization on the structural sidewalls formed by metal-4 as shown on Figure 13(a). The high contrast cross section image of the chip was obtained from a focused ion beam etch. The thickness of the polymer sidewall layer was around 0.1 µm. This thick polymer was only present on sidewall edges defined by metal-4. Sidewall edges defined by other lower-level metal layers did not have significant polymerization. Subsequent dielectric RIE of larger 25 mm^2 chips showed sidewall polymerization on metal-4 edges of as much as 0.3 µm. The presence of the metal-4 or the dielectric layers between metal-4 and metal-3 had a role in the polymerization, but the exact cause is not yet known. The sidewall polymerization is believed to be related to the aluminum loading in the plasma seen previously for wafer-scale processing. A sub-dicing to reduce the chip area to below 6 mm^2 resulted in sidewalls relatively clear of polymer, with no more than 50 nm of polymer present. A photoresist masking of the aluminum in the field also resulted in sidewalls clear of polymer. It was discovered that a lower-level metal enclosure of metal-4 of as little as 1 µm resulted in polymerization next to the metal-4, but not extending onto the sidewall edge defined by the lower-level metal. Therefore, a design rule having the metal-4 cut-in by 1 µm also solved

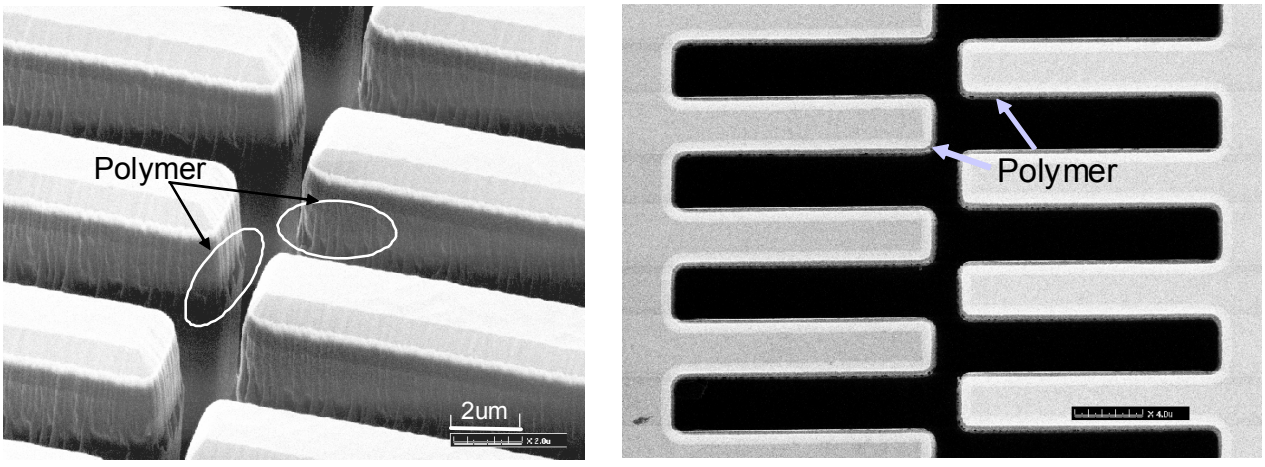
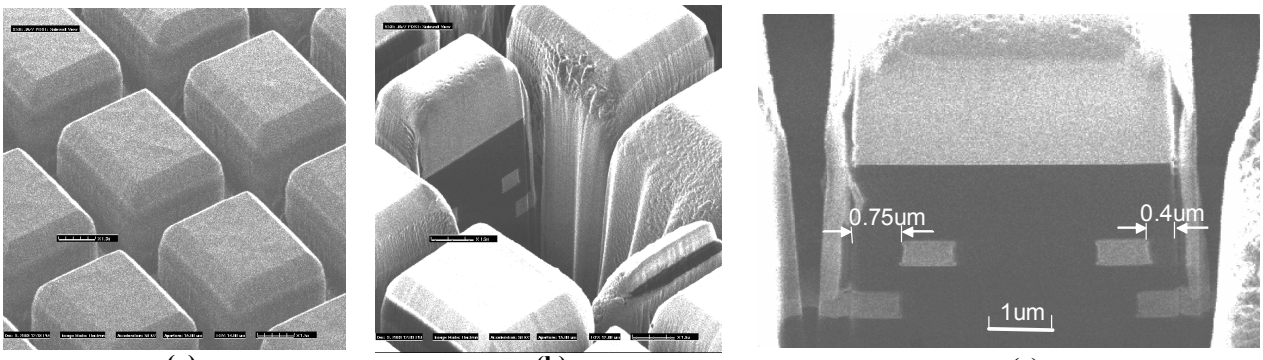


FIGURE 13. SEM images showing (a) sidewall polymerization and (b) structural bloat.



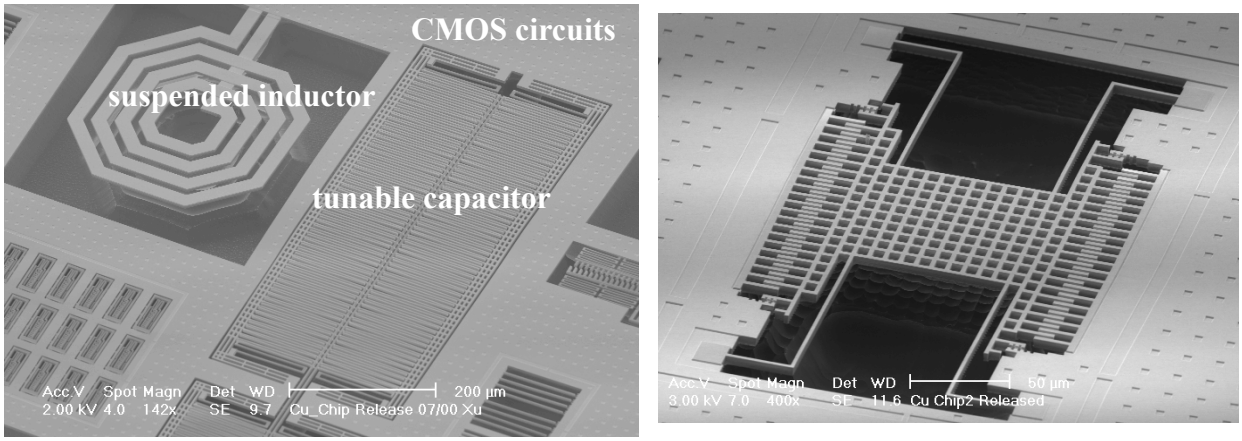
(a) (b) (c)

FIGURE 14. Characterization structure of an array of posts. (a) After post-CMOS processing and before FIB cut. (b) Result of the FIB cut. (c) Enlarged FIB image identifying offset.

the polymerization issue, at the expense of reduced critical dimensions for the microstructures.

The top layer of metal (i.e. metal-4) bloated by about 0.15 µm per side relative to the layout. Figure 13(b) shows a Focused Ion Beam (FIB) image after oxide etch. It shows disengaged comb-fingers from a RF MEMS variable capacitor design [3][4][5]. For small gap design, the fingers can not engage due to the combination of structural bloating and the polymerization formation on the sidewall. In thisparticular design the finger width as laid out was 2.6 µm and the finger gaps as laid out was 0.6 µm. The characterized structure after the oxide reactive ion-etch post-foundry micromachining step led to 2.9 µm wide fingers and 0.3 µm gaps.

The misalignment between metallization layers was measured for a characterization structure of a post array made from a layout of metal-4 squares, shown in Figure 14. The image in Figure 14(a) shows the chip immediately after post-foundry dielectric etch. A FIB cut into this array is shown in Figure 14(b). A zoom in of the FIB cut, viewed with a 45° angle is shown in Figure 14(c). The lower-level metal structures were designed to be symmetrically indented from the edge of the metal-4 layer. The measured indentation is shown in Figure 14(c), and indicates a relative misalignment of about 0.15 µm between these metal layers. A micromechanical structure made with a stack of metal-4 and the lower-level metal layers would be 0.15 µm wider and gaps would be 0.15 µm narrower with this offset. The combination of misalignment, bloat and polymerization, resulted in as-drawn 1 µm-wide air gaps being fused together.



(a) (b)

FIGURE 16. Examples of microstructures fabricated in a 6-metal low-k dielectric copper CMOS process. (a) Voltage-controlled oscillator with tunable MEMS capacitor and suspended inductor. (b) Crab-leg resonator with measured resonance at 31.7 kHz.

Post-CMOS micromachining of Cu and low-k dielectric.

As a side effort to the core ASIMPS project, initial trials of post-processing die with copper interconnect in low-k dielectric were accomplished [6][7]. The ASIMPS oxide etch recipe led to corrosion of the copper surfaces when exposed to air, as shown in Figure 15. To overcome this, the O_2 flow rate was increased from 16 sccm to 25 sccm, keeping the CHF_3 flow rate same at 22.5 sccm. In addition to reducing the resulting corrosion, this recipe reduced the delamination between the low-k dielectric and copper layers forming the micromechanical structures. The 6-layer copper process resulted in a 7.2 µm tall structure. The copper is more resistant to the RIE process as only 0.2 µm of the top copper layer was milled away as compared to 0.5 to 0.7 µm for an aluminum mask layer. Three example microstructures in the copper process were the micromachined tunable capacitor, the suspended copper inductor, and the crab-leg resonator shown in Figure 16.

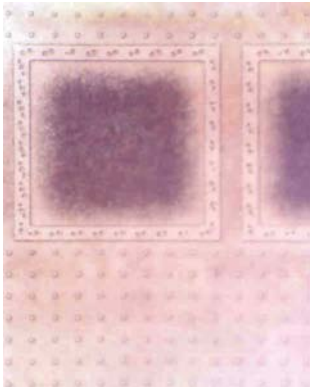


FIGURE 15. A bond pad after two days exposure to the ambient after dielectric RIE showing corrosion on the exposed copper surface.

Silicon DRIE Release Etch Development. The etch lag effect of silicon DRIE anisotropic etch was quantified, because it determines the processing time requirement for different MEMS device designs [8]. The silicon DRIE time required was dictated by the desired amount of spacing from structure to the substrate. Relatively large vertical spacing was desired in past processes to allow clearance for vertical curling due to the residual stress in the CMOS layers. Moreover, this spacing should be large enough to reduce parasitic capacitance from high-impedance sense electrodes to the substrate. Figure 17 shows the etch rate increased linearly with increase of the trench width

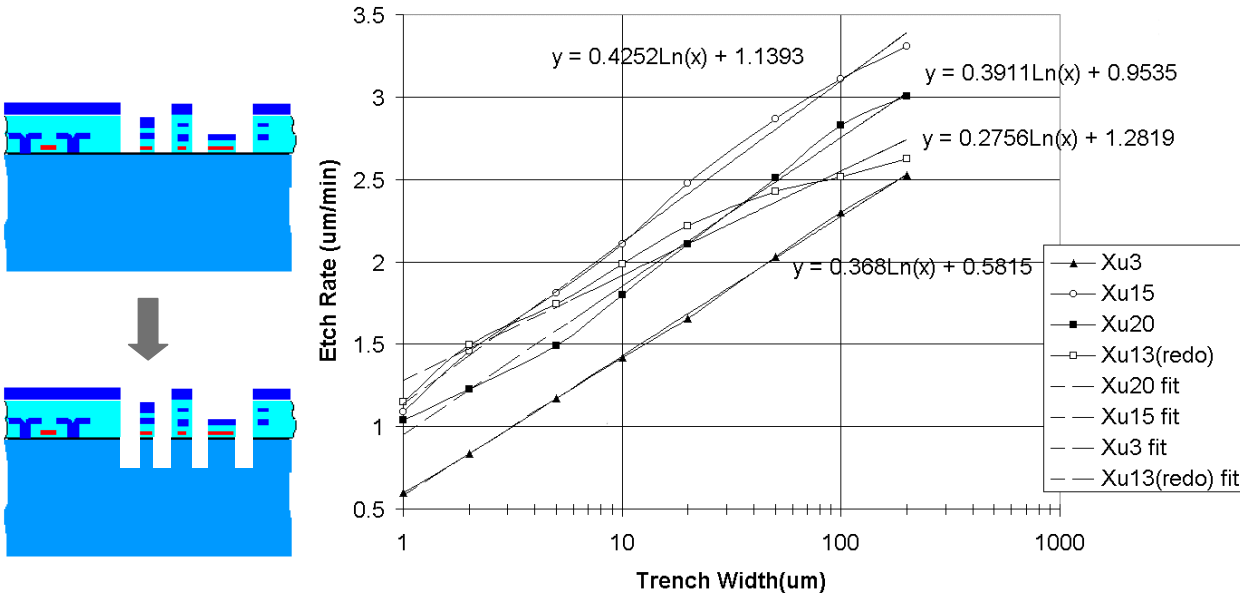


FIGURE 17. The etch lag effect in the DRIE anisotropic silicon etch.

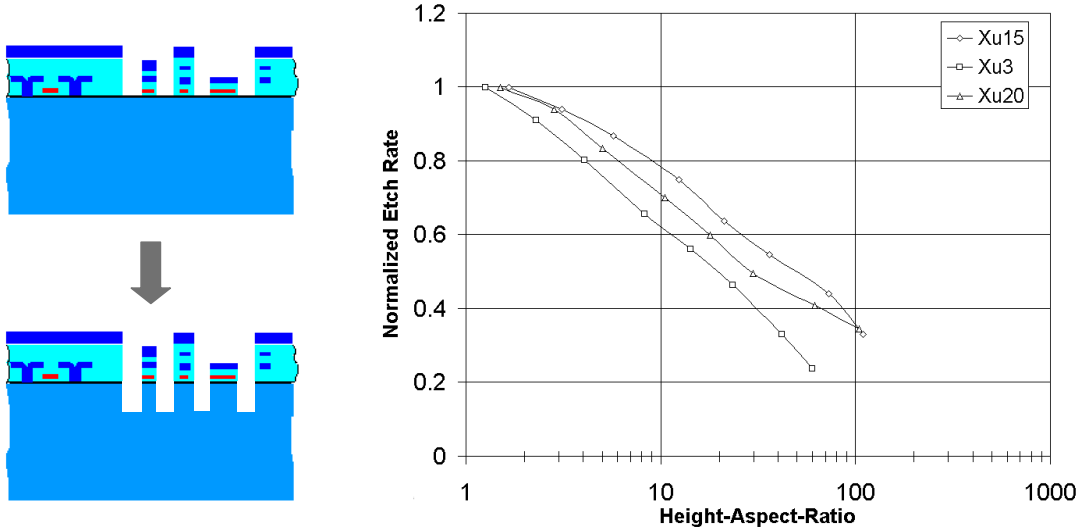


FIGURE 18. The etch lag effect in the DRIE anisotropic Si etch as a function of trench aspect ratio.

with different processing recipes. Very high aspect ratio structures impeded both the transport of etchant species down to trench bottom and the removal of etching by-products. The results of the aspect-ratio dependence are summarized in Figure 18. Isotropic silicon etch rate was characterized to optimize the undercut processing and set values for structural width, hole size and gap design rules. The isotropic etch rates of silicon, shown in Figure 19, were strongly dependent on the hole size. The rates for the fast, medium and slow etch cases varied logarithmically with hole size.

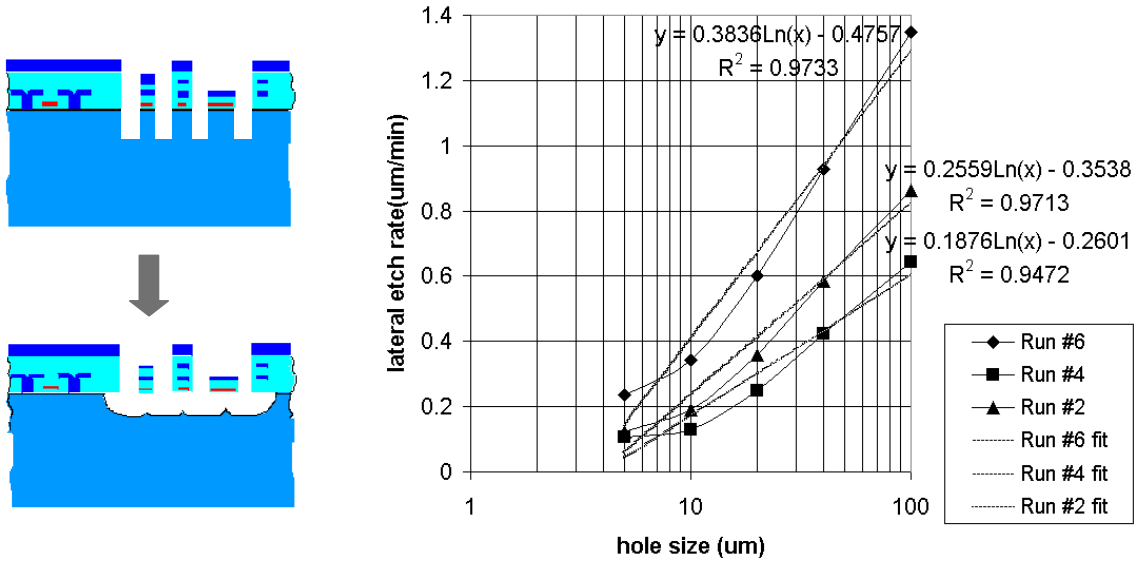


FIGURE 19. The relationship of silicon isotropic etch rates to the hole sizes under fast, medium and slow etch recipe.

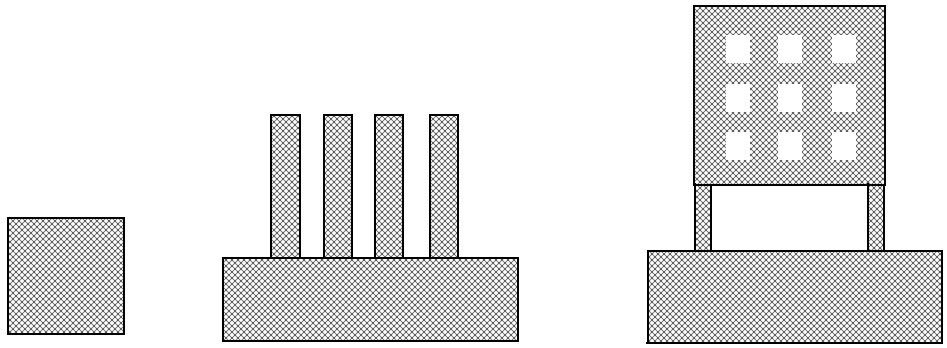
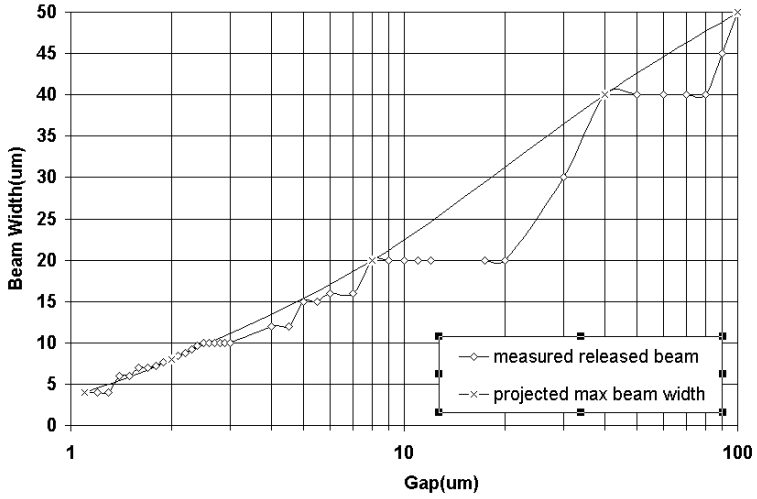


FIGURE 20. Three test structures used for extracting MEMS design rules for post-CMOS micromachining. (a) the square structure. (b) the beam-gap structure. (c) the mesh structure.

Based on this analysis, a set of MEMS design rule check (DRC) verification structures were designed and fabricated. The structures, some of which are shown in Figure 20, included square plates, plates with holes, and beams with surrounding slots. Based on a 5 min isotropic silicon etch, the extracted design rules for the beam, gap and mesh etch are shown in Figure 21. The time related etch depth on the largest opening square space is shown in Figure 22.

Figure 23 summarizes the beam and gap design-rule characterization experiments. After release, the beams were characterized using a Wyco/Veeco white light interferometer. Unreleased beams could be distinguished from released beams from the absence or presence of curl. Silicon etch release recipes of 3, 5, and 7 minutes resulted in expected release characteristics, as shown in the plot in Figure 23(b). The results were uniform across three chips in each release experiment.

(a)



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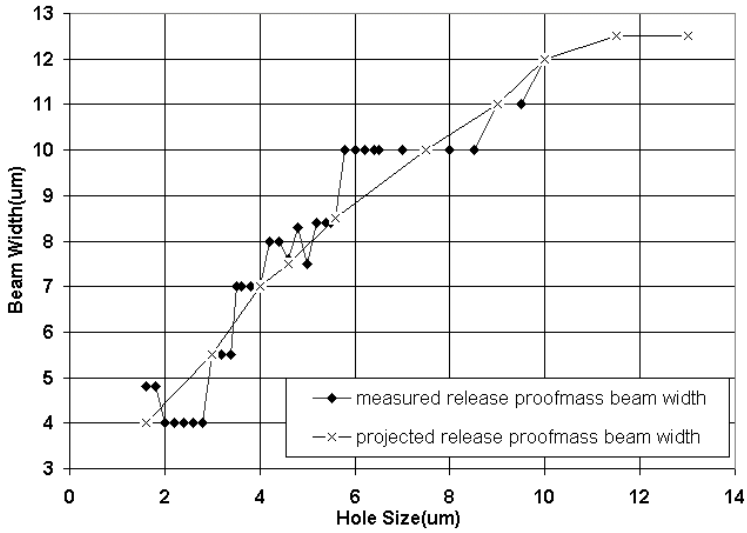


FIGURE 21. Two test structures used for extracting MEMS design rules for post-CMOS micromachining. (a) the beam-gap structure. (b) the mesh structure.

Figure 24 shows the results of characterization experiments on plates as a function of hole size and truss width (i.e., hole-to-hole spacing). The white light interferometer was again used to detect vertical curl. The trend was roughly linear tracking of released truss width to hole size. The "predicted" trend was generated from scattered data points on prior designs. The new measurements of the etch front come from a single set of test structures with better coverage of the design space and are thus far more reliable as future design guidelines. The apparent sudden jumps in etch fronts on the plots are a consequence of too few test structures to completely cover the design space. As with the beam structures, the release data was uniform across 3 chips at each time.

Aluminum Exposure During Silicon Release Etch. After the dielectric micromachining etch was complete, the release steps comprised a 30 min anisotropic silicon etch followed by a 5 min isotropic Si etch, both in the Surface Technology Systems (STS) DRIE system. STS recommends

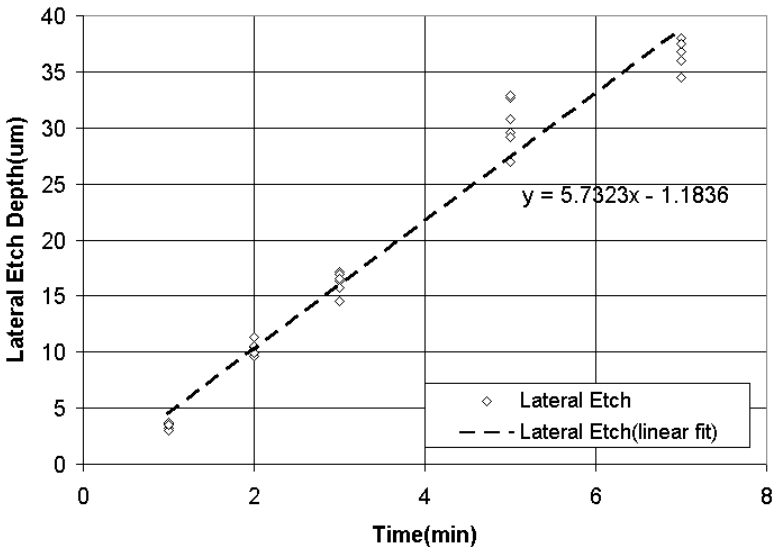
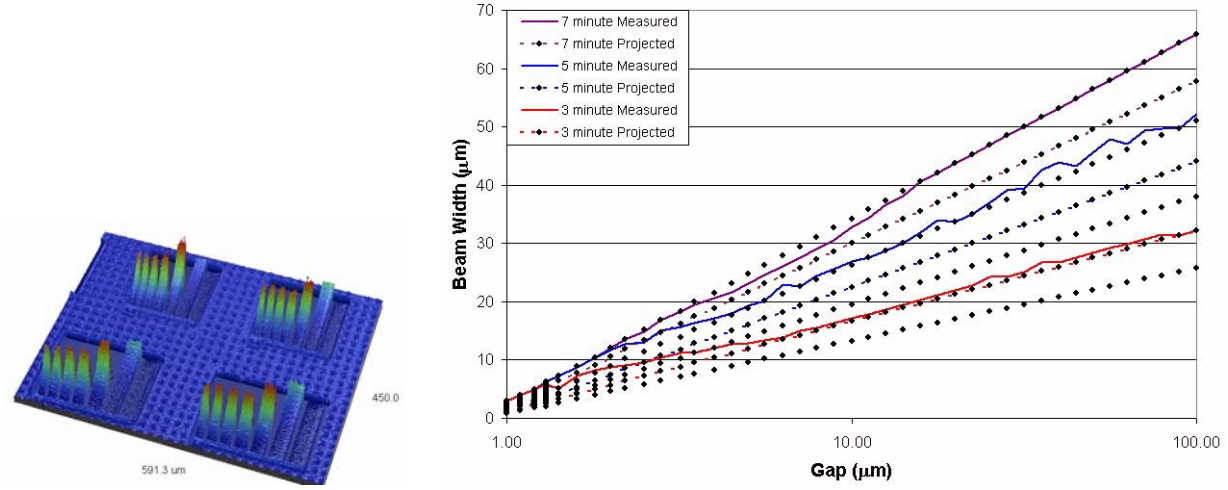


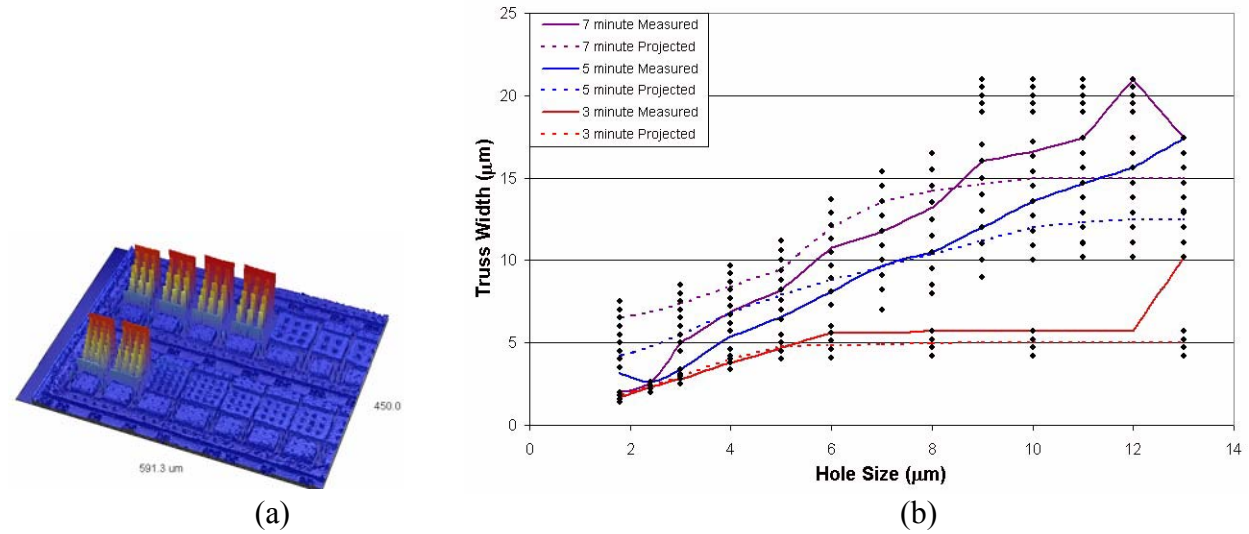
FIGURE 22. Time related lateral etch on a very large opening space.



(a) (b)

FIGURE 23. (a) Interferometric measurement of several design-rule test beams after a 5 minute Si undercut etch. (b) Design rule verification of cantilever beams (dots are test structures, lines are released devices)

that aluminum not be introduced to the DRIE chamber, as it re-sputters over time on the chamber walls and reduces the effectiveness of the inductively coupled plasma. Since the ASIMPS process requires that the top aluminum layer be exposed in the chamber, an experiment to test the short-term effects of aluminum exposure within the STS system was conducted. The experiment was designed to investigate two issues: (1) whether using an aluminum microstructural mask will adversely affect any subsequent conventional silicon DRIE processing, and (2) to quantify the difference between a photoresist mask and an aluminum mask in conventional silicon DRIE processing. Three experiments interspersed with cleaning and chamber conditioning steps were performed:



(a) (b)

FIGURE 24. Interferometer image of DRC plates after 5 minute etch. (b) Design rule verification of plates (dots are test structures, lines are released devices).

(i) The first experiment was to run the standard post-CMOS release recipe first on a photoresist-masked wafer, then on an aluminum-masked wafer, and finally on a photoresist-masked wafer. This compared the effect of two different masks, and determined the effect of the aluminum mask on the subsequent photoresist-masked etch. No significant difference, as indicated in the SEMs in Figure 25, was seen between the two photoresist-masked wafers indicating that there were no deleterious effects from etching a single aluminum-masked wafer. For the standard post-CMOS release process recipe, the measured silicon etch depth with the aluminum mask was 10% less than with the photoresist mask, well within the wafer-to-wafer variation.

(ii) Next, the above experiment was repeated for the standard silicon DRIE shallow trench etch. The aluminum masked wafer and photoresist masked wafers showed the same behavior, other than the fact that the aluminum masked wafer showed almost negligible silicon hillocks.

(iii) The third experiment was intended to identify any longer-term influence of using aluminum masked wafers in DRIE chamber. The aluminum masked wafer was placed in the chamber for progressively increasing amounts of silicon etch time. The system etch rate was monitored to quantify any system degradation over time. The graphs in Figure 26 show etch rate of a normal wafer and shallow recipe silicon etch rate on the aluminum trench mask wafer. There was no major change in the etch rate for 18 hr of etching with aluminum mask exposure. The initial shallow trench etch rate on the photoresist masked wafer was 1.53 µm/min. After the continuous 18 hr aluminum masked wafer etch interspersed with five short etches to check system performance (as in Figure 26(a)), and a 1 hr chamber condition etch, the system etch rate was 3.4 µm/min and the etch rate of the shallow etch recipe on the photoresist masked wafer was 1.36 µm/min. These values are within the run-to-run variation in system performance.

Discussions with Dr. Franz Laermer, Section Manager of Microsystems Technology at Bosch and one of the developers of the Bosch deep silicon etch process, indicated that using this process

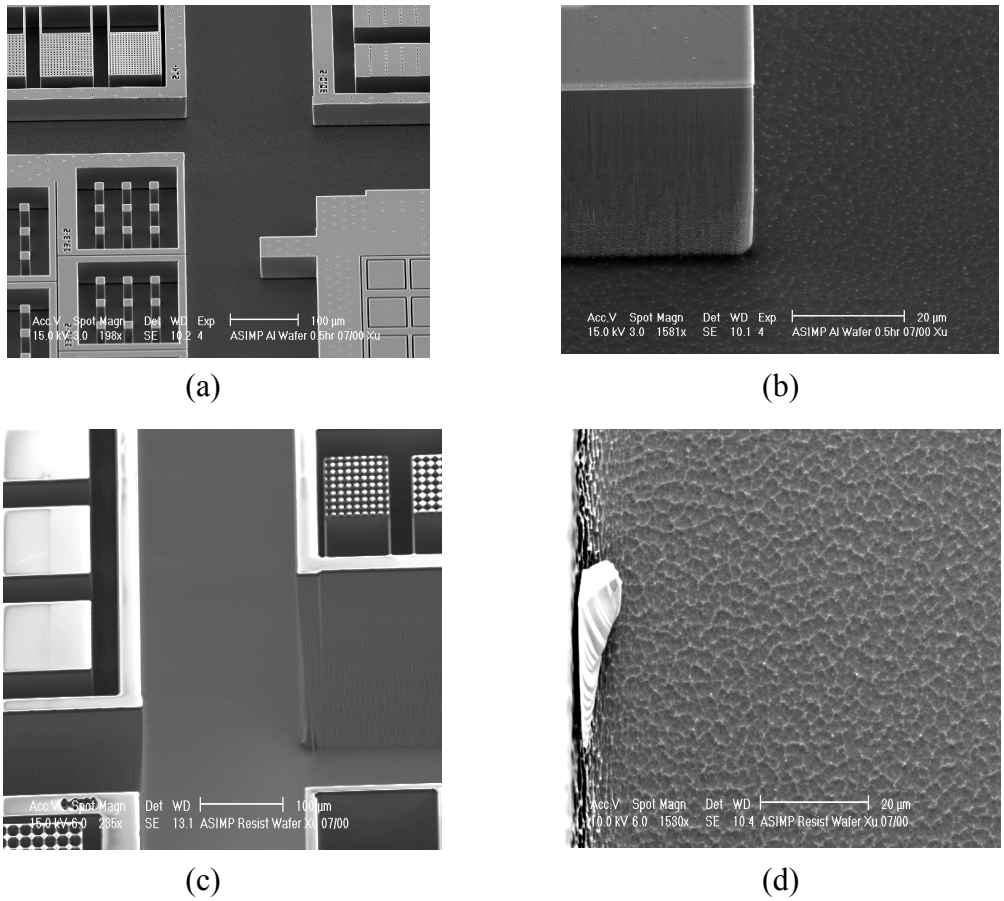


FIGURE 25. Comparison of Al-mask and PR mask in standard post-CMOS release process. Al mask wafer (a) & (b) with 0.5 hr run, and (b) is zoom in of (a). PR mask wafer (c) & (d) with 3 hr run, and (d) is zoom in of (c).

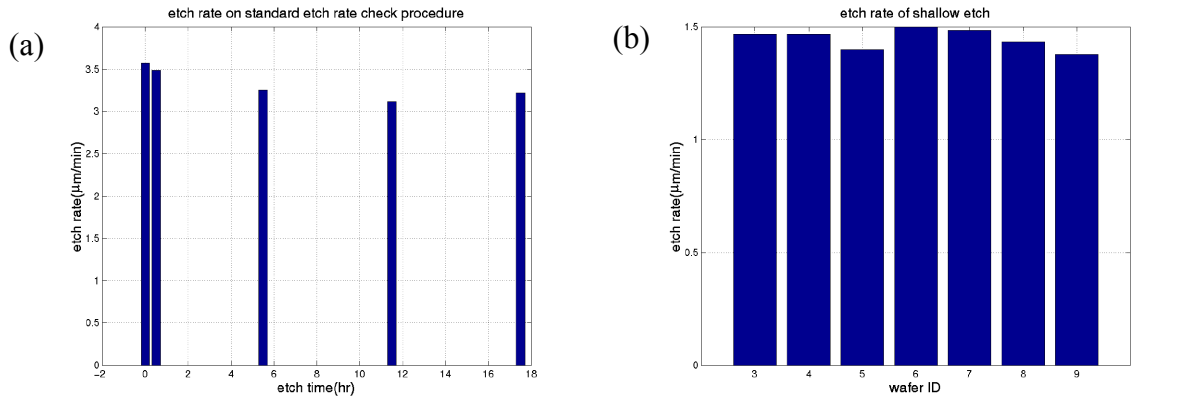


FIGURE 26. (a) System etch rate with photoresist test pattern and (b) etch rate of shallow etch recipe with aluminum mask.

at a manufacturing scale does lead to accumulation of aluminum on the chamber walls. However, regular periodic cleaning of the chamber (in our case, approximately annually) with a mixture of hydrochloric acid and nitric acid is all that is needed to prevent such accumulation.

Silicon needles, shown in Figure 27, form on the bottom surface of the aluminum masked wafer for etch times greater than 2.5 hr. It is hypothesized that these silicon needles result from a micro-masking effect of re-sputtered aluminum or due to a change in the plasma composition from aluminum exposure. The processing pressure was monitored during the run, and showed a variation of less than 5%. The chamber pressure at the beginning and end of the etch process of the aluminum mask wafer and photo resist mask wafer are shown in Figure 28. The etch rate on the aluminum mask due to the shallow trench recipe could not be obtained exactly. It is definitely below 1.8Å/min.

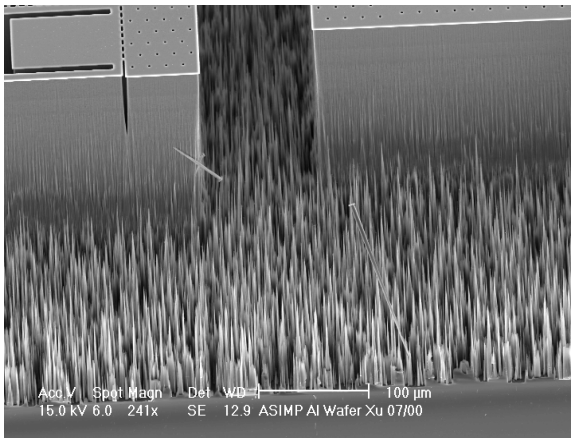


FIGURE 27. Silicon needles generated on the bottom surface.

Bulk Silicon CMOS MEMS Process. A process was refined that combines the maskless post-CMOS micromachining process with a back-side etch to create suspended single crystal silicon (SCS) microstructures integrated with CMOS [9][10]. The deep anisotropic back-side RIE was

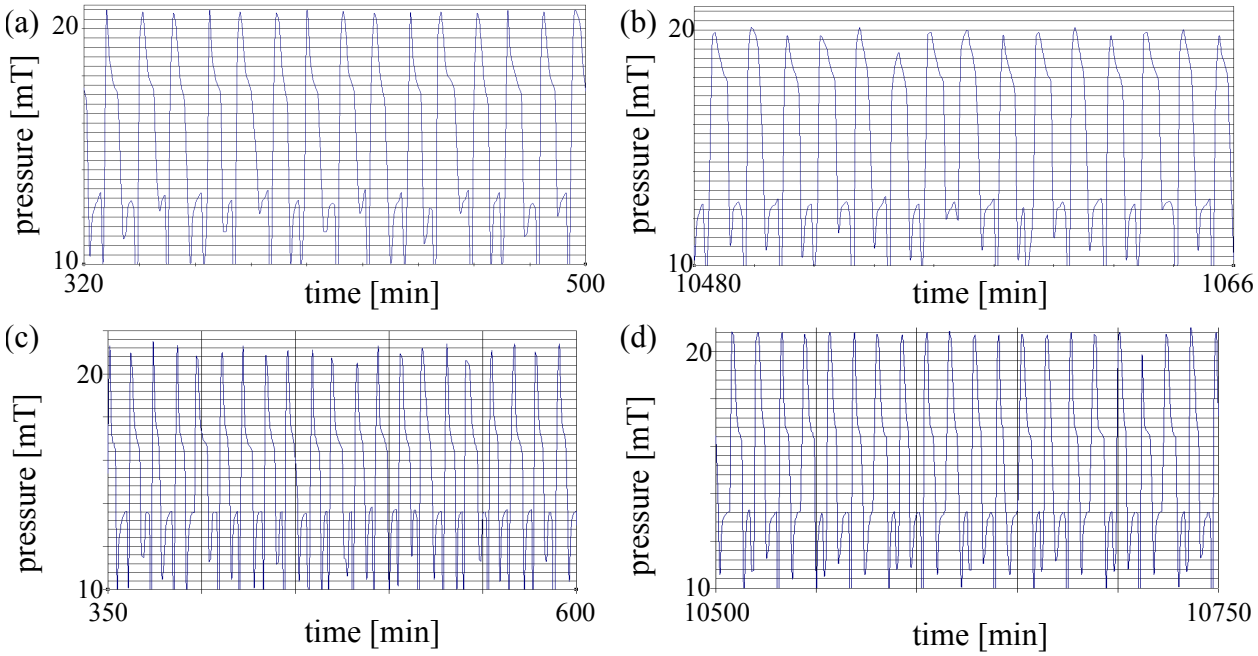


FIGURE 28. Monitoring of chamber pressure of a 3 hr etch on the aluminum mask wafer and the photoresist mask wafer. (a) at the beginning of Al mask wafer. (b) at the end of Al mask wafer. (c) at the beginning of photo resist mask wafer. (d) at the end of photo resist mask wafer.

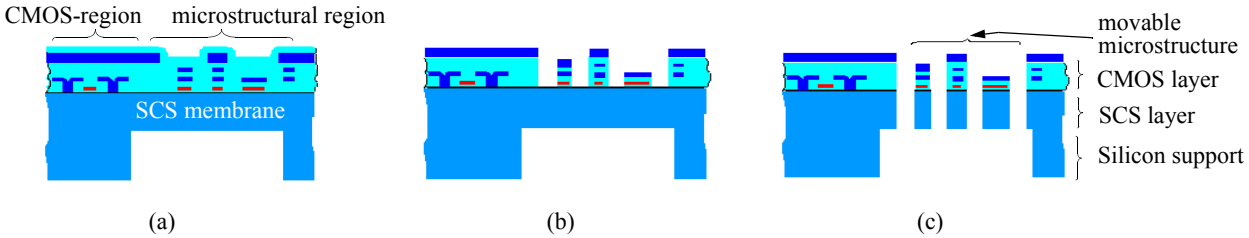


FIGURE 29. The process-flow for the modified CMOS micromachining. (a) CMOS-chip with backside etch. (b) Anisotropic dielectric etch. (c) Anisotropic silicon etch for release.

used to control the thickness of the final, released, microstructures, leaving a 10 to 100 µm-thick SCS membrane (Figure 29 (a)). The silicon frame remaining on the back side provided a support that could be bonded to a package after all processing was completed. Next, a directional dielectric RIE is performed from the front side down to the silicon substrate (Figure 29 (b)). As in the thin-film post-CMOS micromachining process flow, the CMOS metal layers define the structural design. The last step is a timed silicon deep RIE, also from the front side, which is run until the SCS membrane is completely etched through to create released SCS microstructures (Figure 29 (c)). An isotropic silicon etch is an optional additional step (not shown), if narrow metal/dielectric beams are desired. A thick SCS layer remains underneath the CMOS layer, resulting in a very flat released microstructure. The process sequence incorporated the advantages of CMOS composite microstructures with the excellent mechanical properties of single crystal silicon.

Test Structures. Test structure designs to obtain material properties, electrical properties, release process tests, and MEMS design rule characterization were completed early on in the project. The specific cell descriptions are arranged in Table 2 into four categories: material property, electrical, process, and MEMS design rule test structures.

Table 2: Test Structures

Measurand	Description	Layout Cell	Parameters	Cell Description [units in µm]
1.0 Material Property Test Structures				
Axial residual stress (bent beam test)	Axial residual stress of different layer combinations extracted from optical measurement of bent-beam strain.	axstress_a	metal layers {m1, m2, m3} active layer {active} n-diff layer {ndiff} polysilicon layer {poly}	(7) all m321 combinations
		axstress_b		(7) exclusive poly m321p combinations
		axstress_nofox_a		(7) as axstress_a, with active/ndiff layer
		axstress_nofox_b		(7) as axstress_b, with active/ndiff layer
		axstress_polyrel		(7) as axstress_a, with polysilicon release layer (i.e. poly under structure)

Table 2: Test Structures

Measurand	Description	Layout Cell	Parameters	Cell Description [units in µm]
Vertical and lateral stress gradient	Stress gradient extracted from curl. Vertical curl measured with interferometer. Lateral curl measured optically. Three cantilevers: left beam has internal metal offset to left side, center beam has no offset, right beam has offset to right side.	stressgrad	metal layers: spacing between beams {w_g}, width top layer (i.e. of the beam) {w_t}, metal width under layers {w_l}; active layer {active} n-diff layer {ndiff} polysilicon layer {poly}	(21) all m321p combinations {w_g = 9.9, w_t = 2.1, w_l = 0.9} m321p {w_g = 9.9, w_t = 2.1, w_l = 1.5} {w_g = 9.9, w_t = 1.8, w_l = 1.2} m321 {w_g = 9.9, w_t = 2.1, w_l = 2.1} {w_g = 9.9, w_t = 2.1, w_l = 1.5} {w_g = [2.4, 1.2], w_t = 2.1, w_l = 0.9} {w_g = 9.9, w_t = 1.5, w_l = 0.9}
		stressgrad_nfox		(21) as stressgrad, with active/ndiff layer under the beams
		stressgrad_polyrel		(10) all m321 combinations {w_g = 9.9, w_t = 2.1, w_l = 0.9} m321 {w_g = 9.9, w_t = 2.1, w_l = 2.1} {w_g = 9.9, w_t = 2.1, w_l = 1.5} {w_g = 9.9, w_t = 1.5, w_l = 0.9} with poly layer
Effective Young's modulus for lateral motion	Young's modulus extracted from lateral resonant frequency of cantilever beams	youngmod_struct	metal layers: beam length {l_b} beam width {w_b} active layer {active} n-diff layer {ndiff} polysilicon layer {poly}	(15) {w_b = 1.2, 1.5, 1.8, 2.1, 2.4, 2.7, 3.0} for all m321p combinations {l_b = 100}, m321p {lb = 120}
		youngmod_nofox		(14) {w_b = 1.2, 1.5, 1.8, 2.1, 2.4, 2.7, 3.0} for all m321p combinations {l_b = 100}, with ndiff layer
		youngmod_polyrel		(8) {wb = 1.2, 1.5, 1.8, 2.1, 2.4, 2.7, 3.0} all m321 combinations {lb = 100}, with poly layer m321 {l_b = 120}, with poly layer
Mass density	Density extracted from resonant frequency of cantilever beams with plates at ends	dynamic	metal layers	(14) all m321p combination
		static	metal layers	(14) all m321p combination
Effective Young's modulus for vertical motion	Young's modulus extracted from vertical resonant frequency of cantilever beams	z_modulus_str	beam length {l_b} active layer {active} p-diff layer {pdiff}	(56) {l_b = 150 to 420 step 10.0} with and without active/pdiff

Table 2: Test Structures

Measurand	Description	Layout Cell	Parameters	Cell Description [units in µm]
"Fan" cantilever with notched base for crack failure	Stress reliability assessed by notch crack propagation from large resonance of fan	failure_fan	active layer {active} n-diff layer {ndiff} polysilicon layer {poly}	(2) with active/ndiff, with poly
Crab leg resonator	Demonstration test structure of MEMS operation	crab_resr	teeth gap width {w_g} active layer {active} n-diff layer {ndiff} polysilicon layer {poly}	(3) without layers, with active/ndiff, with poly {w_g = 1.2}
		crab_resr_large		(3) without layers, with active/ndiff, with poly {w_g = 1.5}
2.0 Electrical Test Structures				
Polysilicon to m1 contact and metal-to-metal layer via connection	Connectivity verified through resistance measurement. Various size metal cut-out around contacts and vias	4pt_via_noun	metal enclosure of via {w_m} (upper and lower metal) via {via, via2}	(6) via {w_m = 0.4, 0.5, 0.6, 0.7, 0.8, 0.9}
		4pt_via_noun2		(7) via {w_m = 1.2, 1.5, 1.8, 2.1, 2.4, 2.7, 3.0}
		4pt_via2_noun		(6) via2 {w_m = 0.4, 0.5, 0.6, 0.7, 0.8, 0.9}
		4pt_via2_noun2		(7) via2 {w_m = 1.2, 1.5, 1.8, 2.1, 2.4, 2.7, 3.0}
		4pt_via_min	upper metal encl. or via {w_m} (lower metal w_m = 0.4) via {via, via2}	(5) via {w_m = 0.4, 0.5, 0.6, 0.7, 0.8}
		4pt_via2_min		(5) via2 {w_m = 0.4, 0.5, 0.6, 0.7, 0.8}
		4pt_poly_min	upper metal encl. of via {w_m} (polysilicon encl w_p = 0.4)	(7) w_m = 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0
		4pt_poly_min2		(9) w_m = 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.7, 1.8
	tests functioning of via connections	via_series	via {via, via2} number of vias metal encl. {w_m = 0.4}	(1) via - 2, 10, 20, 50 via2 - 2, 10, 20, 50
Meander electrostatic actuator (2)	Serpentine cantilever with alternating electrodes for "squeeze-in" actuation	self_act	active layer {active} n-diff layer {ndiff} polysilicon layer {poly}	(3) without layers, with active/ndiff, with poly
3.0 Process Test Structures				

Table 2: Test Structures

Measurand	Description	Layout Cell	Parameters	Cell Description [units in µm]
Profilometer layer step thickness (1)	Thickness of metal layers with profilometer	alpha_step	metal layers	(1) m321p, m21p, m1p, p, none, m1, m2, m3
Resistive silicon undercut	Extarct undercut resulting from etching by measuring resistance increase of n+ diffusion resistor	restrstr_und_layout	gap width {w_g} Etch holes on both sides of diffusion (two-sided), one only one side (one-sided), and no etch holes (none, which is the control)	(10) two-sided {w_g = 1.5, 1.6, 1.7, 2.0, 2.5, 3.5, 6.5, 12, 22} one-sided {w_g = 12} none (reference structure)
Vertical electrostatic actuator (10)	test Z-axis movement	ztest_str	mass dimensions{dim} active layer {active} n-diff layer {ndiff}	(10) {dim = 3.6, 4.8, 6.0, 7.2, 9.6} with and without active/ndiff
SEM studs and studs for focused-ion-beam cross-sectioning(FIB studs)	Short cantilever beam stubs, located on edge of die allowing for SEM photo to to measure stack thickness and beam width. Varying gaps to assess affect on sidewall profile	gap_1_6	gap widths {w_g} beam width {w_b = 3.0} m321	(1) {w_g = 1.0, 1.2, 1.5, 1.8, 2.1, 2.4, 2.7, 3.0, 3.3, 3.6, 3.9, 4.2, 4.5, 4.8, 5.1, 5.4, 5.7}
		gap_6_13p5		(1) {w_g = 6.0, 6.6, 7.2, 7.8, 8.4, 9.0, 9.9, 10.8, 11.7, 12.6, 13.5}
		gap_13p5_20p7		(1) {w_g = 13.5, 14.7, 15.9, 17.1, 18.3, 19.5, 20.7}
		gap_21_29p4		(1) {w_g = 21, 23.1, 25.2, 27.3, 29.4}
		sem_studs1	gap widths {w_g} beam width {w_b} m321 polysilicon layer {poly}	(1) for w_b={1.5, 2.1}, {w_g = 1.0, 3.0, 10.0} with and without poly
		sem_studs3	metal layers	(1) all m321p combinations
	varying metal combinations next to each other in a row	sem_studs2	metal layers active layer {active} n-diff layer {ndiff}	(1) all m321p combinations, with and without active/ndiff
	see effect of violating m3 slotting rule	sem_studs_m3	m3	(1) dimensions 37.1 x 397.0
Beam structures	test for release of beams with varying gap	beam_gap_DRIE	gap width{w_g}	(31) {w_g = 10 to 40 step 1.0}

Table 2: Test Structures

Measurand	Description	Layout Cell	Parameters	Cell Description [units in µm]
Squares	measure undercut etch rate with comparison of doping effects	square_layout_row_pcl	square dimension {d_s} gap width {w_g} active layer {active} n-diff layer {ndiff} p-diff layer {pdiff} n-well layer {nwell}	(~195) $w_g = 4 * d_s$, {d_s = 3.0 to 4.9 step 0.1} $w_g = 3 * d_s$, {d_s = 5.0 to 9.9 step 0.1} $w_g = 2 * d_s$, {d_s = 10.0 to 14.9 step 0.1} $w_g = d_s$, {d_s = 15.0 to 30.0 step 0.2} over four quadrants (no doping, active/ndiff, active/pdiff, active/nwell)
Beam matrix	Check release of beams based on varying distributed gap width and beam width combinations	beam_matrix_a	beam width {w_b} gap width {w_g}	(25) {w_b = 2.0, 2.5, 3.0, 3.5, 4.0} for {w_g = 1.0, 1.1, 1.2, 1.3, 1.4}
		beam_matrix_b		(25) {w_b = 4.0, 5.0, 6.0, 7.0, 8.0} for {w_g = 1.3, 1.4, 1.5, 1.6, 1.7}
		beam_matrix_c		(25) {w_b = 6.5, 7.25, 8.0, 8.75, 9.5} for {w_g = 1.6, 1.8, 2.0, 2.2, 2.4}
		beam_matrix_d		(25) {w_b = 8.0, 9.0, 10.0, 11.0, 12.0} for {w_g = 4.0, 4.5, 5.0, 5.5, 6.0}
		beam_matrix_e		(25) {w_b = 10.0, 12.5, 15.0, 17.5, 20.0} for {w_g = 8.0, 9.0, 10.0, 11.0, 12.0}
Beams with tapered sidewalls	tests curling of beams based on combinations of metals	tapered_beams	metal layers and beam widths	various metal combinations
4.0 MEMS Design Rule Test Structures				
Beam release with gap width	Check release of beams based on initial MEMS DRC rules	gapwidth_str	gap width {wg}	(20) 1.5, 3.0, 6.0, 10 each +/- 10%, +/- 20%
Basic beam release	Check release of beams based on MEMS DRC rules	basic_beams	beam width {w_b} gap width {w_g}	(5) {w_b, w_g}: {1.5, 1.2}, {3.3, 1.5}, {6.0, 2.1}, {10.0, 5.0}, {20, 10}
Metal enclosure of polysilicon	measure minimum enclosure of poly to beam edge; offset accounted by measuring enclosure on one side at a time	poly_space_str_pcl	poly enclosure {encl} offset orientation {+/- x/y} active layer {active} n-diff layer {ndiff}	(6) {encl = 0, 0.3, 0.5, 0.6, 0.7, 0.9} for no offset (with and without ndiff), offset without ndiff for {+x, -x, +y, -y}

Table 2: Test Structures

Measurand	Description	Layout Cell	Parameters	Cell Description [units in µm]
Metal-to-metal structural cut-in	Check minimum cut-in required for continuous beam	cut_in_structure	metal layers cutin {w_{cut}} orientation {+/- x/y}	(3 x 4) m32, m31, m21 {w_{cut} = 0, 0.1, 0.2, 0.3, 0.4, 0.5} {+x, -x, +y, -y}
Beam curl/ width	minimum width for beams to avoid "excessive" lateral curling	beam_curl_row_pcl	metal layers beam widths {w_b} gap width {w_g = 10.0} n-diff layer {ndiff}	(50) all m321p combinations {w_b = 1.2 to 1.9 step 0.1, 2.0 to 2.8 step 0.2, 3.0 to 4.2 step 0.3, 4.6, 5.0 to 8.0 step 0.5} with and without ndiff
Via spacing	(see above in 2.0 Electrical Testing)			

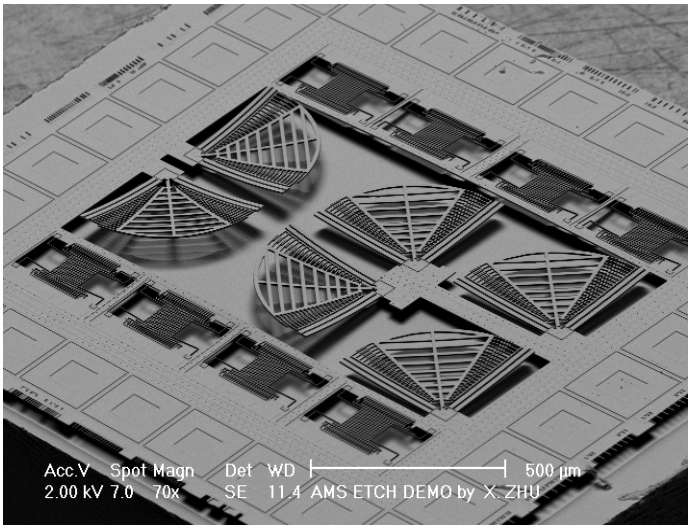


FIGURE 30. Released AMS chip containing 6 resonant fan structures made of various CMOS dielectric and metal layers. Eight crab-leg comb-drive resonators are present along the periphery of the chip. The devices without field oxide under them show the least vertical curl.

These test structures included measurements to extract axial residual stress, residual stress gradient, lateral and vertical Young's modulus, and mass density. Simple demonstrator devices such as a crab-leg resonator and a failure "fan" structure [11] (shown in Figure 30) were also included. Several contact and via test structures were designed to verify operation after the CMOS-MEMS dielectric etching and silicon release etch. Process test structures included diffusion resistor structures to measure the undercut from the release etch, vertical actuators and step structures to measure layer thickness, and short cantilever stubs for SEM and FIB cross-section imaging. MEMS design rule test structures included beams with varying surrounding gaps and plates with varying etch holes to characterize the necessary gaps and holes necessary to guarantee device release, as was discussed earlier. Structures were made to determine the safe oxide enclosure around polysilicon, which is vulnerable to the silicon release etching.

For the Jazz process, 125 µm long cantilever beams with 5 µm by 5 µm plates at their ends

were used to extract the effective Young's Modulus (approximately 100 GPa for metal-4 beams, 85 GPa for metal-3 beams, 75 GPa for metal-2 beams and 63 GPa for metal-1 beams) and density (approximately 2400 kg/m^3 for metal-3 beams). Residual stress was extracted using a bent-beam structure. Since the residual stress is dependent on the layers in the beam, data from combinations of the metals in the Jazz process were extracted. The stress ranged from 1 MPa to 10 MPa with the exception of metal1/poly and metal2/poly beams which had residual stresses of 0.1 MPa. Vertical curl arising from the residual stress gradients in the multi-layer structure sets the limit of the largest structure that can be designed without curl compensation. As with the other CMOS micromachining processes, the removal of field oxide reduced the curl, with structures that have all 4 metals and the active mask having radius of curvature larger than 18 mm. In fact, with the field oxide removed, all the beams except the metal1-only beam had a radius of curvature that exceeded 2 mm (the nominal size of an ASIMPS chip).

4.2 ASIMPS Design Support and Development

During the course of the project, five short courses were held July 20 and 21, 2000, March 26 and 27, 2001, and January 10 and 11, 2002, May 1-2, 2003, and in May 2004. The following institutions attended the short courses: AFRL Rome, Benchmark Photonics, Berkeley Sensor and Actuator Center, Bosch Palo Alto, Carnegie Mellon, Carnegie Mellon Robotics Institute, Cronos, The Corporation for National Research Initiatives (CNRI), George Washington University, IBM Research Division, Johns Hopkins' Applied Physics Laboratory, MEMSCAP, Motorola's Radio Products Group, SPAWAR, Tyco, and Xactix. Additionally the short course materials were provided to Analog Devices, Morgan Research and MIT, and Unmanned Systems Technologies.

The short courses did not include any generic MEMS background material, instead focusing directly on the ASIMPS post-CMOS micromachining process. The course was partitioned into three half-day sessions aimed at rapidly traversing the learning curve involved in CMOS MEMS design. The first half-day session presented the top issues a MEMS designer needs to know to become a successful CMOS MEMS designer. The second half-day session involved a hands on CAD tutorial on the MEMSCAP ASIMPS engineering kit. Tutorial material was developed for designing beams, springs, plate-masses, comb drives, anchors, pads, and post-design slotting. Electronics tutorials to demonstrate the schematic-based design, and extraction-based verification capabilities of the design kit were also developed. Finally, the third-half day session, assisted by the various CMOS-MEMS design experts amongst the students, staff and post-doctoral researchers at Carnegie Mellon was allocated to a custom user design session to kick start the design effort.

An integrated MEMS design methodology that combines the point tools developed in prior DARPA-funded projects on "Foundations for MEMS Synthesis," and "Integrated MEMS Inertial Measurement Unit" [12][13][14][15] was developed for ASIMPS. Screen images of the design environment, based on the commercial integrated circuit design tools from Cadence, are shown in Figure 31. This methodology enables rapid custom design by abstracting from the 3D solid model representation commonly used in the early '90s, and the 2D layout representation used in the mid-1990s to a schematic-centered representation, with tools to obtain the layout representation from the schematic. The MEMS model library enabling the schematic environment is called NODAS,

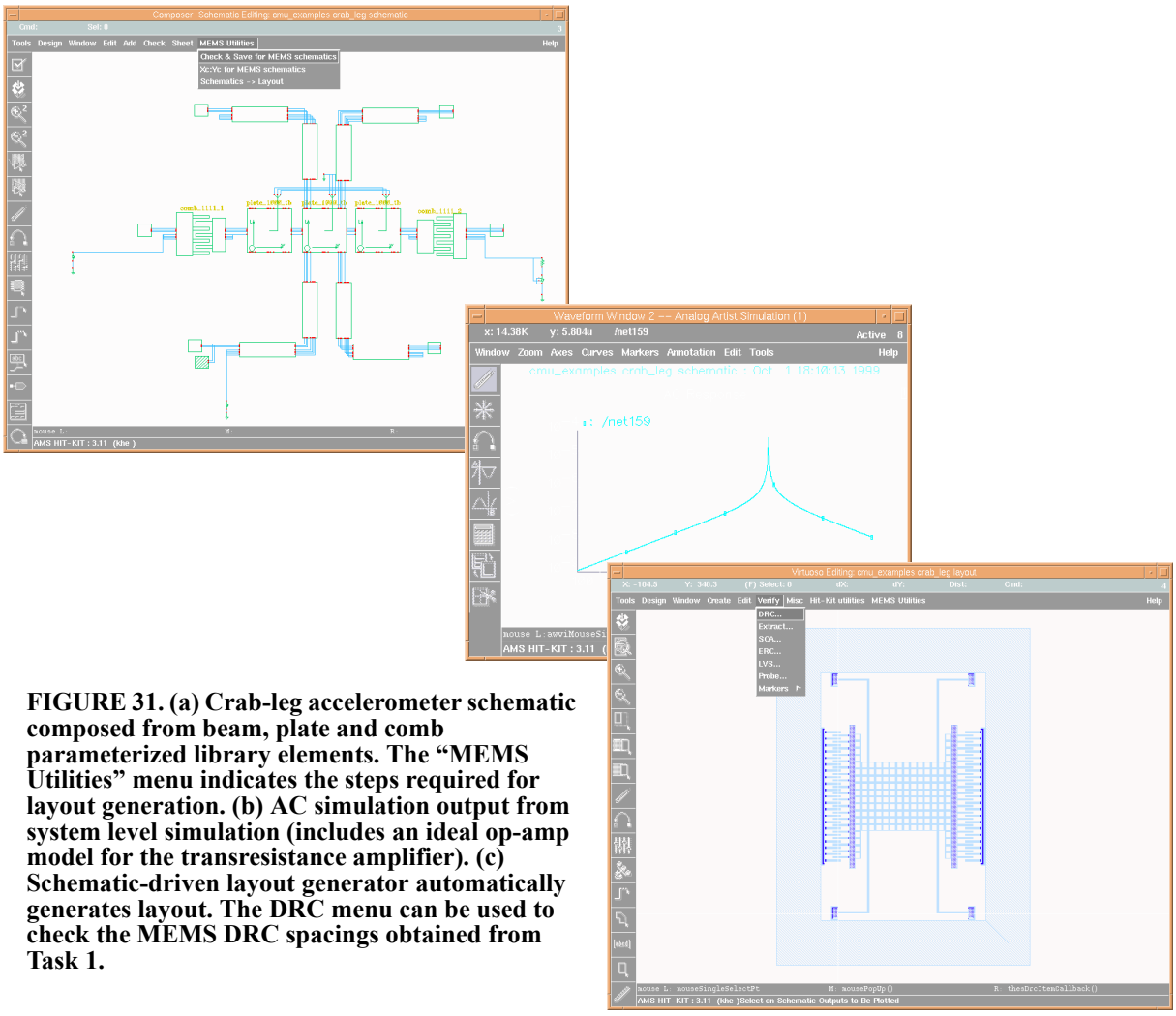


FIGURE 31. (a) Crab-leg accelerometer schematic composed from beam, plate and comb parameterized library elements. The "MEMS Utilities" menu indicates the steps required for layout generation. (b) AC simulation output from system level simulation (includes an ideal op-amp model for the transresistance amplifier). (c) Schematic-driven layout generator automatically generates layout. The DRC menu can be used to check the MEMS DRC spacings obtained from Task 1.

for NOdal Design of Sensors and Actuators. General MEMS designs can be represented by interconnecting composable beam, plate and comb capacitor elements. The details of the models and the model code are available from a Ph.D. thesis [16]. Short-course participants used the NODAS design environment for schematic entry and automatic layout generation to manage the design effort in the multi-electrical layer, single structural layer process. As an example of the potential design productivity, one participant was able to get a 5000 rectangle layout design completed by the end of the 1.5 day short course.

Following the first workshop, MEMSCAP developed the first-generation ASIMPS engineering kit as shown in Figure 32. The kit was based on Cadence's Virtuoso layout software and contained the technology files for the AMS 0.6 µm CMOS process, automated generation of non-Manhattan shapes, a cross-section viewer and a translator between Cadence's layout database and ANSYS for 3-D visualization. In mid 2000, MEMSCAP launched a product called MemsXplorer, which included these new capabilities. A similar kit for the MEMSPro environment was developed for users preferring a lower cost design environment. Similar design support for microma-

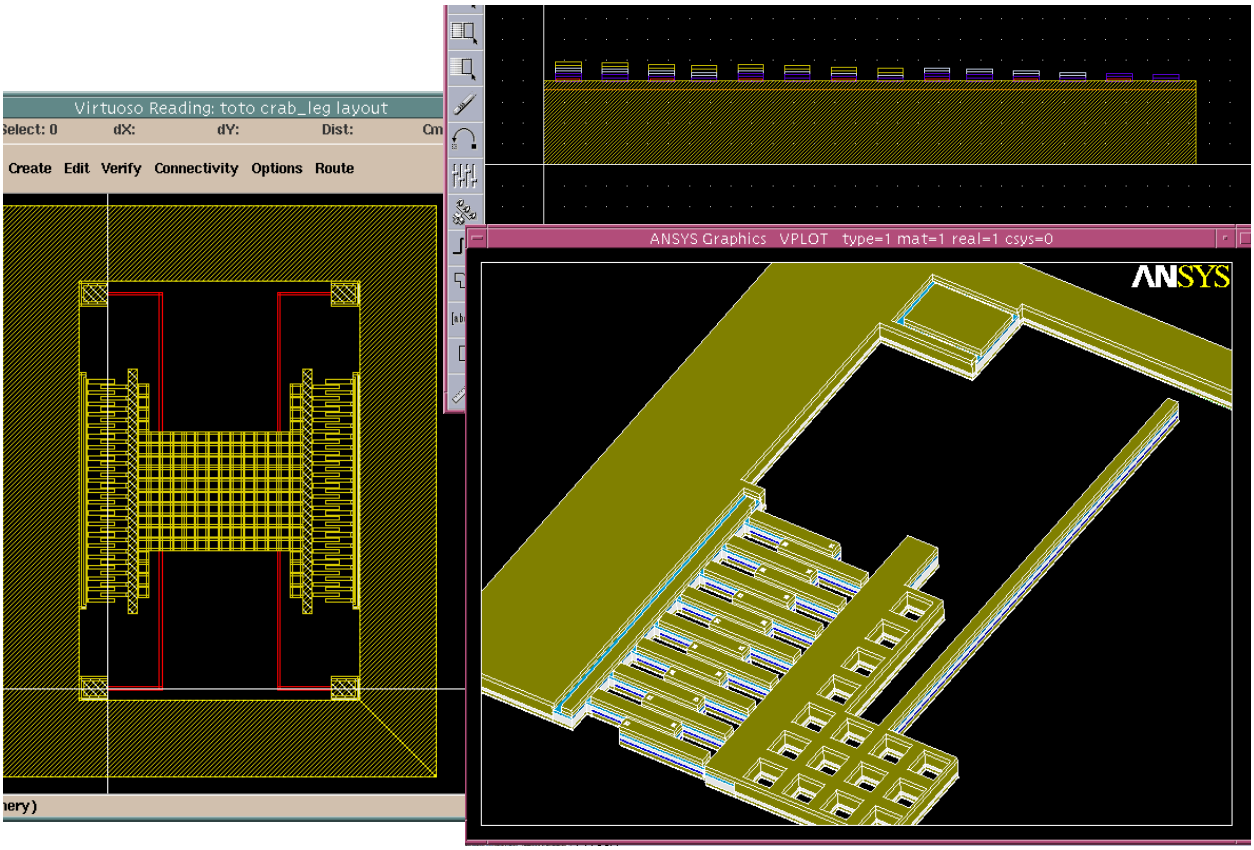


FIGURE 32. Screen shots showing device layout, beam cross-section, and device visualization using MEMSCAP's first-generation ASIMPS engineering kit

chining in the Jazz BiCMOS technology was initiated in 2003 and completed in 2004.

At Carnegie Mellon, research towards improved design environments for MEMS focussed on the schematic representation and layout interface support for ASIMPS. Incremental results on the NODAS model development were documented in several publications [17][18][19][20][16][21][22][23]. Highlights are summarized here.

Linear beam and plate model enhancements. The NODAS 3D linear beam model was expanded to include asymmetric trapezoidal cross-sections defined by two sidewall angle parameters. Verification of the updated 6-DOF (degree of freedom) beam elements was performed by comparing NODAS simulations to finite element analysis (FEA, using the ABAQUS commercial tool) with brick and Euler-Bernoulli beam elements. Tests for coordinate transformation, beam bending and resonance for cantilever beams, fixed-fixed beams and a crab-leg resonator were completed. Table 3 shows the static and AC simulation results for a cantilever beam (100 µm long, 2 µm wide, and 2 µm thick). Displacements and resonant frequencies are listed for each case. NODAS results matched the Bernoulli beam simulations to within 3% and matched brick FEA to within 6%. For f_x and $f_{\theta x}$, errors were around 10% when using only one beam element to represent the cantilever beam. Two beam elements are needed in order to reduce the error to within 6%. The additional error is due to the consistent mass formulation (*i.e.*, using same shape functions for

Table 3: Simulation results of a cantilever beam

	NODAS	*Abaqus (Bernoulli Beam)*	*Abaqus (Brick)*	*error NODAS vs. Beam*	*error NODAS vs. Brick*
d_x (μm)	1.5152e-10	1.5152e-10	1.5153e-10	0	0.01%
f_x (Hz)	21.53M (2 beam) 23.17M (1 beam)	21.04M	21.04M	2.3% 10.3%	2.3% 10.3%
d_y (μm)	1.5152e-6	1.5149e-6	1.5097e-6	0.02%	0.36%
f_y (Hz)	273.17k	271.9k	272.5k	0.47%	0.25%
d_z (μm)	1.5152e-6	1.5149e-6	1.5097e-6	0.02%	0.36%
f_z (Hz)	273.17k	271.9k	272.5k	0.47%	0.25%
θ_x (rad)	6.993e-2	6.993e-2	6.4462e-2	0	8.5%
$f_{\theta x}$ (Hz)	12.3027M (2 beam) 13.1826M (1 beam)	12M	13.05M	2.5% 9.8%	5.7% 1%
θ_y (rad)	4.545e-2	4.5477e-2	4.5106e-2	0.06%	0.8%
$f_{\theta y}$ (Hz)	273.17k	271.9k	272.5k	0.47%	0.25%
θ_z (rad)	4.545e-2	4.5477e-2	4.5106e-2	0.06%	0.8%
$f_{\theta z}$ (Hz)	273.17k	271.9k	272.5k	0.47%	0.25%

mass matrix as for stiffness matrix). Beam models incorporating thermal expansion to model vertical curl were also explored [24][25].

The NODAS rigid plate model was enhanced to allow individual joint-offset parameters for each connection terminal. This provides more generality in defining mechanical connections to the plate. Schematic and transient analysis results of a micromirror verification example are given in Figure 33. AC analysis shows a close match of resonant frequency to FEA to within 2%.

A 3D linear elastic plate model with bending and stretching was implemented. Experiments, summarized in Figure 34, verify that the resonant frequency of plate bending matches FEA to within 2%, and the resonant frequency of in-plane stretching matches FEA to within 8%. The elastic plate model currently has only four connection terminals at corners without joint-offset, and will be expanded to a similar format as the rigid plate model.

Nonlinear beam model. A nonlinear beam model was created that captures the geometric nonlinearity in all six degrees of freedom. The small-deflection geometric nonlinearity model is based on the geometric nonlinear stiffness matrix K_G given by Przemieniecki (*Theory of Matrix Structural Analysis*, McGraw-Hill, 1968). Refinements that use modeling techniques such as force projection and calculation of the effective length of the deformed beam based on beam bending shape functions were used to extend Przemieniecki's buckling beam model for the cantilever beam and guided-end beam. Static analyses were performed to verify the model. Figure 35 shows the simu-

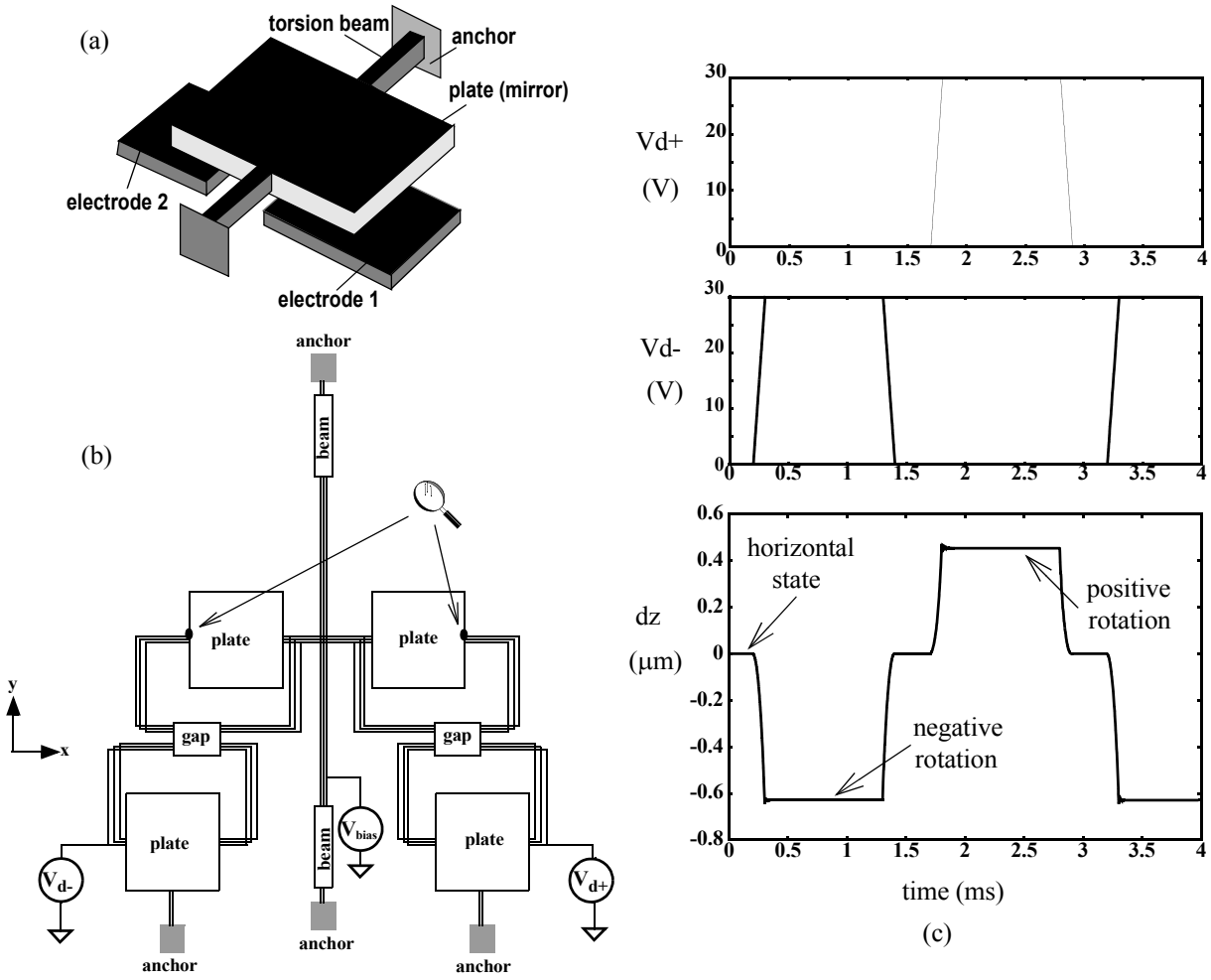


FIGURE 33. Simulation of a micro mirror using 3D linear beam element and 3D rigid plate element (a) Micro mirror (b) Schematic in NODAS (c) Transient analysis in NODAS

lation results for a cantilever beam. Compared to the analytic elastica solution and ABAQUS simulation results, the error of NODAS simulation is less than 10% for beam displacement less than 15% of the beam length. Similar simulation accuracies are obtained for fixed-fixed beams, folded-flexure springs and crab-leg springs.

Elastic plate model. Przemieniecki's stiffness and mass matrices were used to develop a nonlinear elastic plate model that captures both out-of-plane bending and the in-plane stretching of the plate. The element has four terminals at corners, each of them with six nodes representing the translational and rotational through and across variables about *x*, *y* and *z* axes. Figure 36 shows the simulation results for the resonant frequency of the bending mode and the stretching mode. NODAS results match to ABAQUS results to within 10%.

Comb drive model. A methodology for combined regression modeling of capacitance and force in the electrostatic comb with multiple metal layers was developed [26]. Boundary element analyses (BEA) was used to obtain capacitance values for a range of comb finger width, gap, overlap, cur-

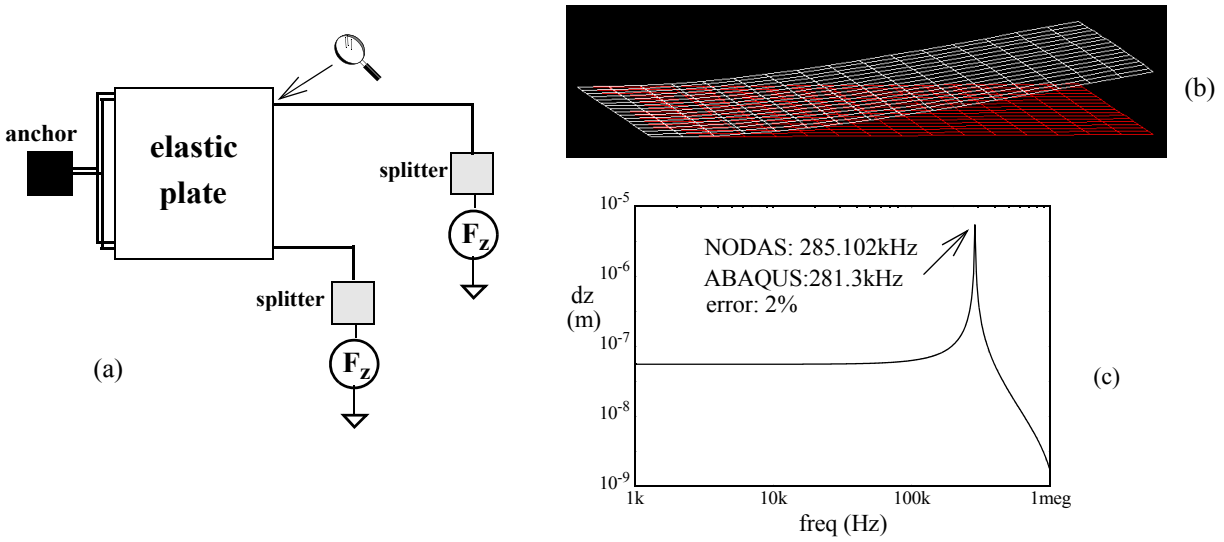


FIGURE 34. Simulation with elastic plate element (a) Schematic in NODAS (b) Mode shape of elastic plate bending (ABAQUS) (c) Frequency response.

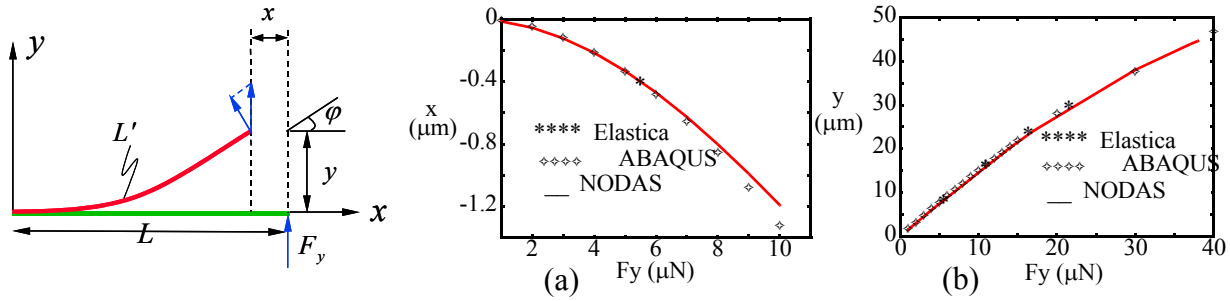
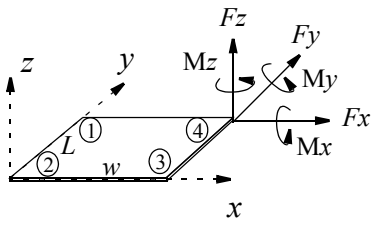


FIGURE 35. Static analysis of a cantilever beam (*L*=100 μm, *w*=2 μm, *t*=2 μm, *E*=165 GPa) under a force in y-direction (a) displacement in x; (b) displacement in y.



		ABAQUS	NODAS (1 plate)	error	NODAS (4 plates)	error
bend	*fz*	281.3 KHz	285.102 KHz	1.4%	283.465 KHz	0.8%
stretch	*fx*	21.17 MHz	23.1739 MHz	9.5%	21.8776 MHz	3.3%
	fy	8.817 MHz	9.33254 MHz	5.8%	9.23240 MHz	4.7%

FIGURE 36. (a) 3-D elastic plate (b) comparison of NODAS and ABAQUS simulation results (*L*=100 μm, *w*=100 μm, *t*=2 μm, *E*=165 GPa).

vature as well as the position and orientation. Self-consistent electrostatic force was found from numerical differentiation of the capacitance values. The mesh used in the BEA for obtaining capacitance values for numerical differentiation was more refined than the mesh used for obtaining the capacitance values used directly for fitting. The number of BEA and the type of data (capacitance and forces F_x, F_y, and F_z) obtained is summarized in Table 4. The times shown are

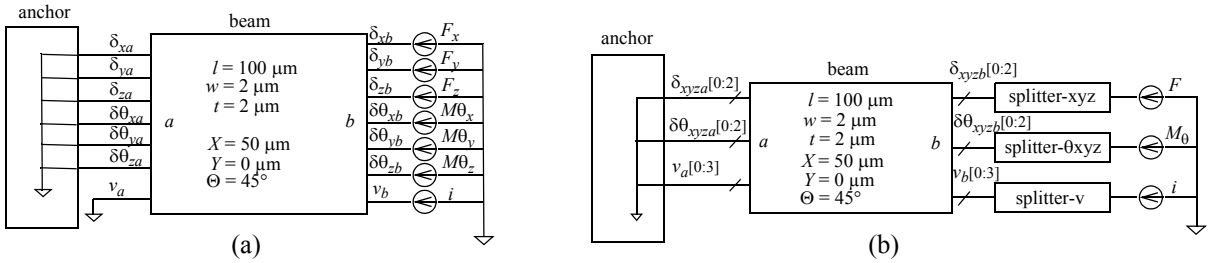


FIGURE 37. NODAS schematic of a cantilever beam on a chip with (a) individual (b) bus pins.

for analyses run on one CPU (central processing unit) of a 450 MHz Sun Ultra-80 workstation. The F_x values were computed using three closely spaced capacitance data points while the F_y and F_z values used a common set of 1458 capacitance values to compute derivatives at 972 points. The runs used to obtain capacitance values for computing forces used higher mesh refinement, and therefore, required higher memory and CPU time.

Table 4: Summary of BEA runs for different quantities

Quantity	Number of values obtained	Total number of BEA runs	No. of BE panels (approx.)	Memory required per run (MB)	Time taken per run (minutes)
Capacitance	n=4374	4374	22000	230	5
F_x	m_x=54	162	90000	850	24
F_y	m_y=972	1458	90000	850	24
F_z	m_z=972	1458	90000	850	24

Bus and Global pins. The effectiveness of this approach is shown in the comparison between a schematic representation of a cantilever beam on a chip in Figure 37. Each port has six DOF to represent the 3-D beam bending and torsion: translational motions along x, y and z axes, and rotational motion about x, y and z axes. These six mechanical pins were reduced to two bus pins by aggregating all the translational and rotational pins into separate bus pins. The current Verilog-A language (and other analog hardware description languages) does not allow cross disciplinary pins, thus three bus pins were used (translational, rotational and electrical) in the updated behavioral models. Bus splitter elements were developed to translate from vector bus to scalar individual pin representations for stimulus application and pin monitoring needs. Global pin support for external acceleration fields applied to all schematic elements on a chip were also developed. Prior to this feature, each schematic element with inertia (plate, beam, comb) required six acceleration wires to distribute the acceleration fields. A secondary issue was that the AHDL syntax does not allow global pins, which was solved by using a hierarchical system schematic to hide the global pins.

Angle Representation. Previously developed 6-DOF beam and plate models had nine angle parameters specifying the direction cosines between the chip-frame and the local frame. This representation was redundant and prone to error during parameter entry by the user. Therefore, the 6-

DOF models were modified to use Euler angles instead of direction cosines. The three Euler angle parameters are α for rotation about the x-axis, β for rotation about the y-axis and γ for rotation about the z-axis. The resulting coordination transformation matrix depends on the order of rotations, requiring a convention. The convention used in NODAS is to first rotate about the z-axis by γ, then rotate about the y-axis by β, and last to rotate about the x-axis by α. This convention was used because rotation about the z-axis (corresponding to a rotation in layout) is the most common case.

Mixed-Domain Extraction. A mixed-domain simulation methodology was established which allowed extraction and simulation of layouts of integrated MEMS and circuits (with parasitic capacitances and resistances) [27][28][29][30][31][32]. This feature allowed designers to evaluate the effect of electrical and mechanical parasitics on the behavior of both the MEMS and circuits. For example, for a CMOS-MEMS accelerometer, the sensitivity of the integrated MEMS and electronics was degraded by 23.5% due to the mechanical and electrical parasitics.

New scanline based algorithms were implemented to achieve $O(n \log n)$ speed crucial for layout extraction of micromechanical and electromechanical elements. For instance, consider an ASIMPS example (from an ASIMPS short-course attendee) of 5000 rectangles. The same micromechanical topology in a polysilicon process involves on the order of 500 rectangles. The primary reason for the larger number of rectangles in CMOS-MEMS is the larger number of metal layers available, which enables arbitrary electrical routing inside the mechanical structure. Extraction of comb drives from layout was implemented through a graph-based approach for the comb-drive recognition algorithm, which is analogous to the previously existing spring recognition algorithms. These graph-based algorithms were written to allow users to specify lists of matching targets in a text file library in order to customize the extractor. The extractor was re-written to allow a user-specified process description file, thereby resulting in a process-independent extractor. The current code can be used to extract structures done in both the AMS ASIMPS and MUMPS processes.

Slotting of metal in the field. A metal-slotting software tool was developed to support ASIMPS. It was applied to slot the designs from the individual participants in the AMS multi-project alpha runs. Slotting of large-area metal regions is required by the CMOS foundry design rule document to prevent peel off due to stress. Initially developed to just slot the metal-3 layer, as this tends to be used as the mask layer for the ASIMPS project, the tool was found to be inadequate for several designs planned for the alpha run. Extensions to handle slot holes with covers in multiple metal

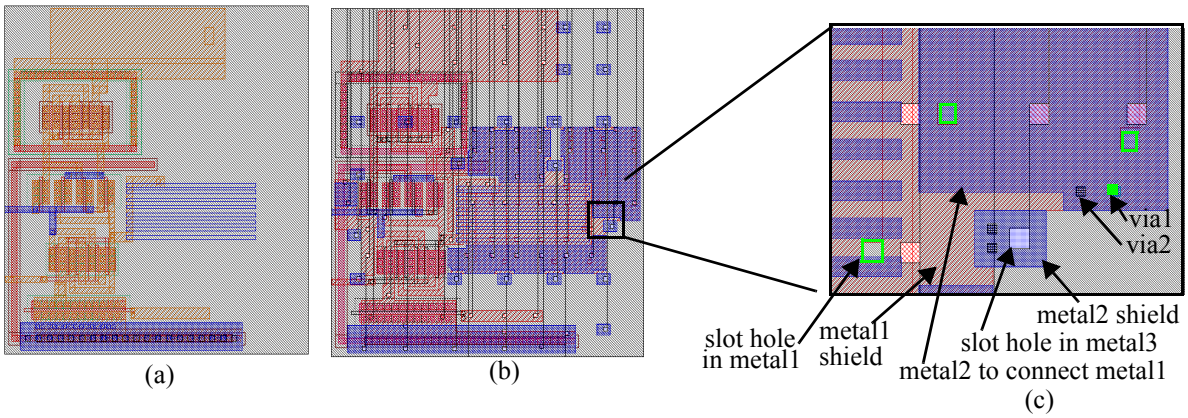


FIGURE 38. Slotting for a buffer circuit; (a) original layout, (b) slotted layout, (c) metal1 and metal2 shields for slot holes

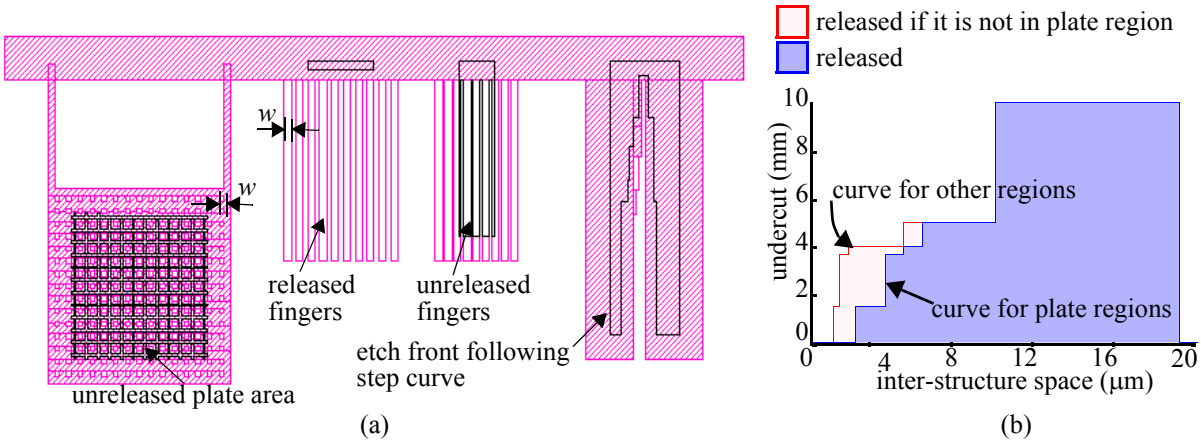


FIGURE 39. (a) Example demonstrating MEMS DRC cases, (b) Graph showing undercut widths for various inter-structure spaces

layers was added. An example of a layout and the result of auto slotter is shown in Figure 38(a) and (b) respectively. Figure 38(c) shows slot covers in metal-2 and metal-1 that were added to act as shields for slot holes added in metal-3. The metal covers added were also slotted if needed. Slot holes were also intelligently added by the slotter in places which already had metal covers (not shown).

In addition to the slotting, improvements in the DRC algorithm included implementing the context dependent nature of ASIMPS DRC more efficiently, as demonstrated in Figure 39(a). The design rule follows one of the two step curves shown in Figure 39(b) depending on whether the gaps lie in plate region or non plate region. The unetched areas are found by emulating the etching process in accordance to the experimentally obtained graph in Figure 39(b).

4.3 ASIMPS Technology Drivers

CMOS-MEMS Infrared Pixel. An infrared pixel was designed, fabricated and tested [33]. The

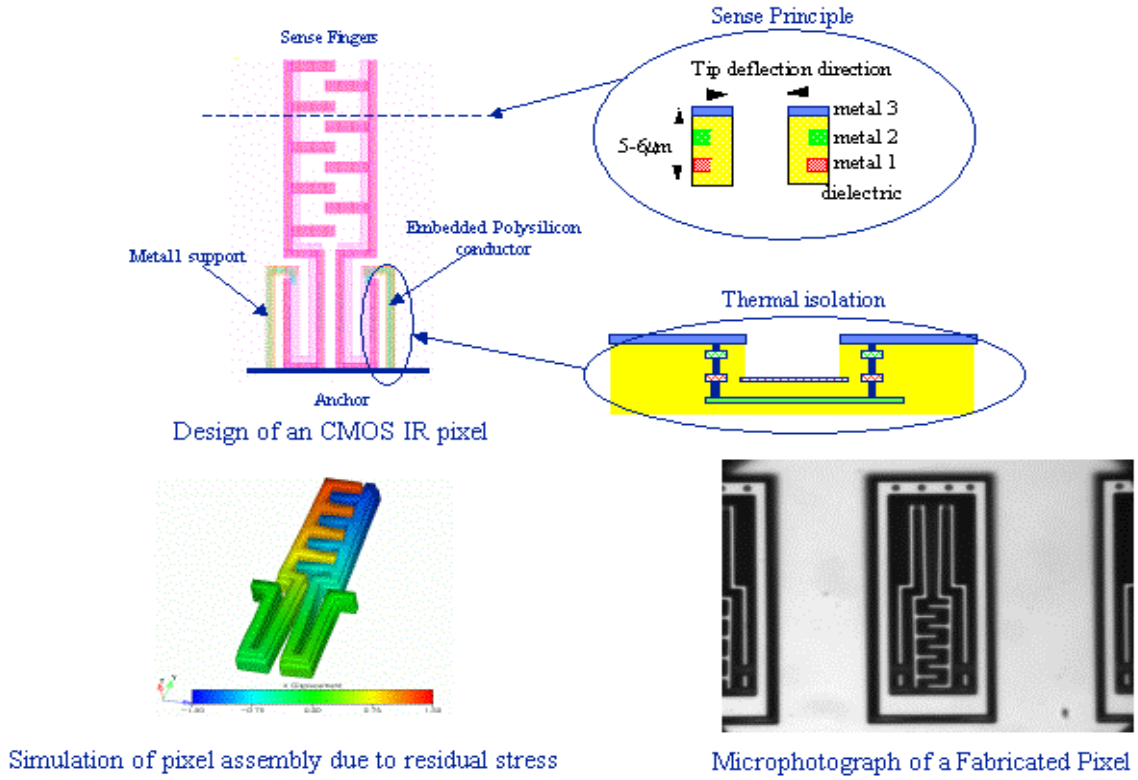


FIGURE 40. CMOS MEMS infrared pixel.

thermomechanical characteristics of the CMOS multi-layer interconnect stack is used to transduce infrared energy into displacement. The displacement is sensed capacitively using the sense fingers shown in Figure 40. The measured sensitivity of the pixel was 0.57 mV/K with a noise floor of 6 mK/rtHz. Details regarding this pixel can be found in [33].

Accelerometer Synthesis. The philosophy behind ASIMPS is to involve the application expert in integrated MEMS design. As such, experts are not likely to be MEMS designers and toolkits to ramp up their design capabilities are needed. One such toolkit is a layout synthesis tool for ASIMPS accelerometers [34]. The synthesis tool is an extension of the original DARPA Composite CAD funded "Foundations on MEMS Synthesis" efforts on accelerometer synthesis. Four accelerometers whose layout was synthesized automatically were fabricated in the first alpha AMS run to verify the synthesis design tool. They involved designs optimized for (i) minimum noise, (ii) maximum sensitivity, (iii) minimum area, and (iv) maximum range. Following the CMOS foundry fabrication, the devices were placed through post-CMOS micromachining at the die-level, then packaged and wire bonded.

As this was the first alpha run, the designs were primed using material properties measured for previous HP 0.5 μm runs. The results from these devices are summarized in Figure 41. The measured resonant frequencies, measured optically using the MIT MicroVision system, are within 10% of the expected values. The measured noise was 5.4 mG/rtHz for the minimum noise device

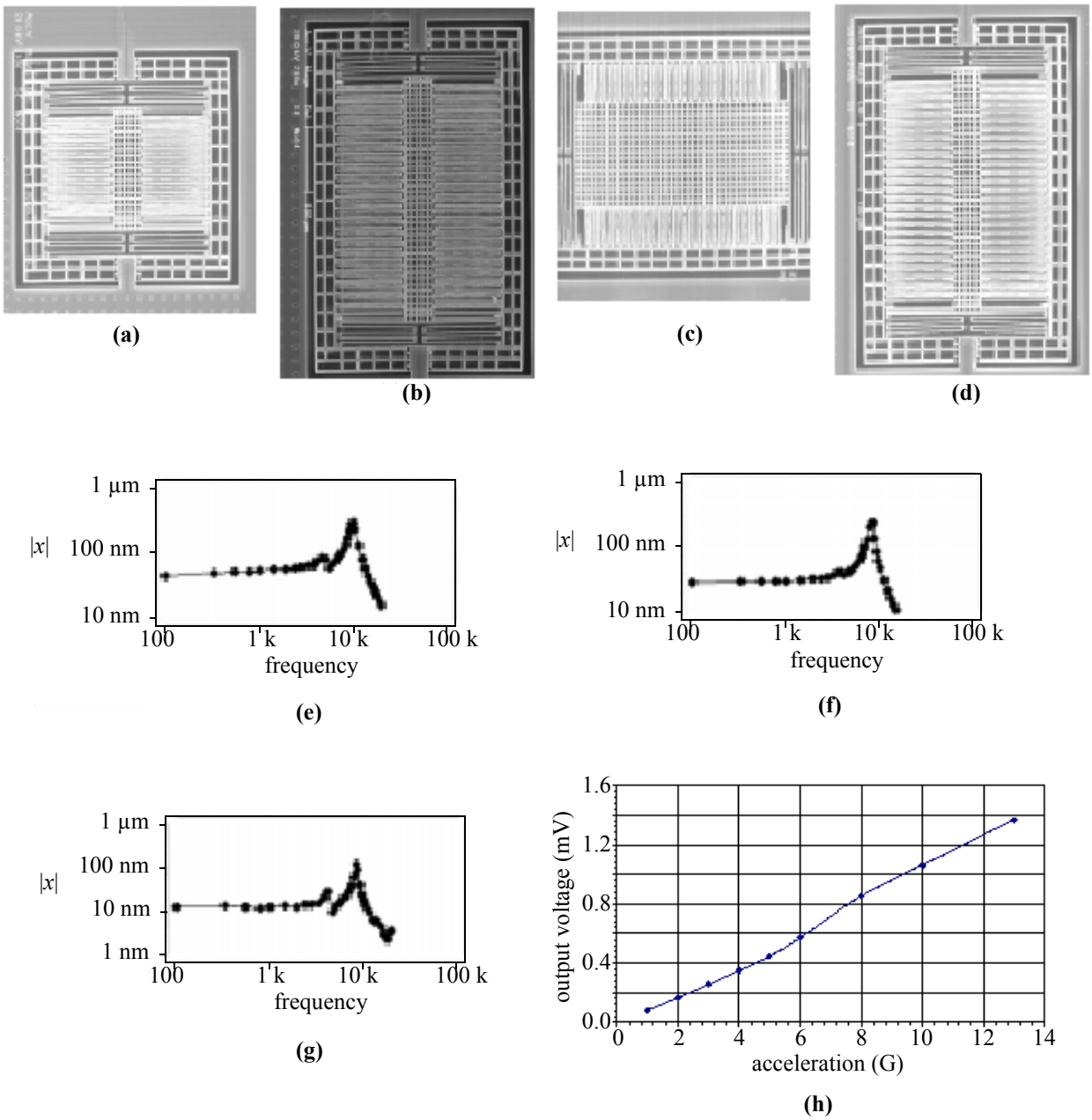


FIGURE 41. SEM of released synthesized (a) minimum area, (b) minimum noise (c) maximum sensitivity and (d) maximum range devices. The optically measured device mechanical response of the primary axis of optimized (e) area, (f) noise, (g) range devices; and (h) dynamic linearity of range accelerometer.

and 14.9 mG/rtHz for the maximum range device. The AMS ASIMPS devices exhibited high residual stress gradients (both lateral and vertical), thereby degrading the expected performance of the synthesized devices. The maximum sensitivity device was not operational due to excessive lateral curl (as thin beams were used by the synthesis tool to ensure a compliant spring and thin gaps were used for increased ΔC/C).

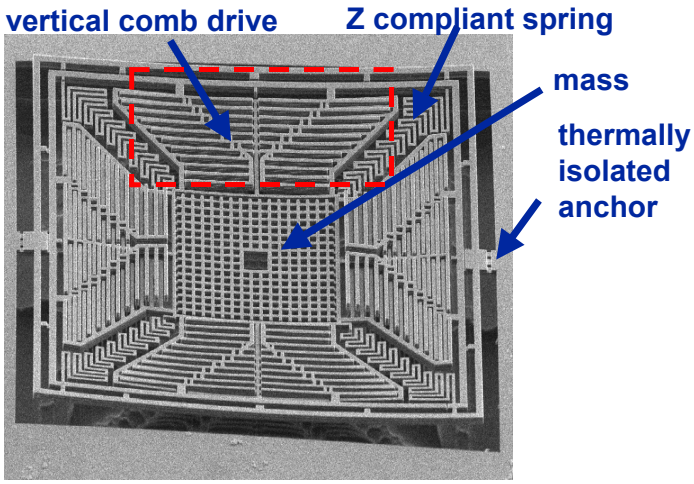


FIGURE 42. The z-axis accelerometer designed to test the thermal stabilization principle. Polysilicon heater resistors are embedded in the proof mass, the surrounding stator frame, and the rotor comb drive.

Thermally stabilized accelerometer. One important consideration in designing microstructures made using the metal and the dielectric layers in ASIMPS is the presence of residual stress gradients, that cause structures to curl out of plane and in plane. Curl matching structures helped improve nominal device performance for the synthesized accelerometers. However, due to the large difference in thermal expansion coefficients of the aluminum (23 μ/K) and the oxide (0.4 μ/K) layers, the curl is function of temperature. The out-of-plane curl can cause variation in output offset and sensitivity of CMOS micromachined capacitive sensors. The situation is complicated by the dependence of in-plane curl variation with temperature due to misalignments of the metal masks during the foundry CMOS fabrication.

A temperature compensation technique was explored that aims to keep the temperature of the device constant using integrated polysilicon resistors of the CMOS process embedded in the device structure [35][36]. Keeping the device at a constant temperature rather than keeping the entire chip at a fixed temperature leads to lower power consumption and reduces packaging difficulties. A z-axis accelerometer sensitive to out-of-plane acceleration was used as a test-bed for demonstration of the temperature control scheme. A SEM of the accelerometer design is given in Figure 42. The accelerometer motion was sensed by a vertical comb drive designed by controlling the rotor and stator curvature. The polysilicon layer of the CMOS process was utilized for heating the device structure to a constant temperature, higher than the highest operating temperature. The capacitance detection circuits had temperature independent gain.

The major results of offset and sensitivity improvements are given in Figure 43. In the z-axis accelerometer, the average rotor temperature was controlled at 90 ºC, and the stator was controlled at 130 ºC. The total power required to heat the device was about 100 mW at room temperature and 40 mW at 85 ºC. The output offset stability of the accelerometer improved from 1.9 G/°C, to 42 mG/°C, and the sensitivity stability improved from 60% to 18% over a temperature of 70 °C after temperature control. The dc output variation was reduced to 3 G over a 70 ºC temperature range. These results are not impressive when compared with commercial accelerometers,

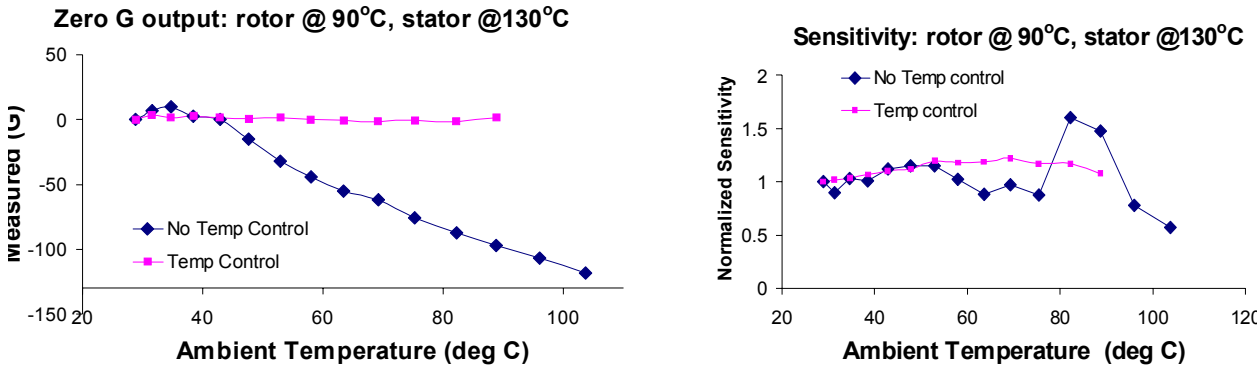


FIGURE 43. Temperature stabilization results for the z-axis accelerometer offset and sensitivity vs. ambient temperature.

however, the testbed accelerometer was purposefully designed with a large curl effect. The thermal control principle is expected to provide an improvement of better than 20x for offset and 20% for sensitivity for any CMOS-MEMS capacitive sensor.

Accelerometers. Several accelerometers and gyroscopes were fabricated using ASIMPS or ASIMPS developed processes. Several of these devices were designed under the DARPA sponsored Integrated MEMS Inertial Measurement Unit project. The first-generation of CMOS-MEMS lateral-axis accelerometers achieved around 1 mg/$\sqrt{\text{Hz}}$ noise floor, limited by electronic noise [37]. An interface circuit with a periodic bias reset provided an improvement in noise floor [38].

The most recent generation of CMOS-MEMS accelerometer within the DARPA ASIMPS project was completed in 2004 and had measured mechanical Brownian noise-limited resolution of 45 µg/$\sqrt{\text{Hz}}$ at 1 atm [39]. An accelerometer micromachined from the 4-metal TSMC 0.35 µm CMOS process, is shown in Figure 44. Similar accelerometers were also designed in the Jazz Semiconductor 4-metal 0.35 µm SiGe BiCMOS process with identical topology and similar transducer sizing. A modified pre-amplifier design with sub-threshold transistor dc biasing was found to be robust against leakage paths to positive and negative supplies and had an input referred noise of 14.6 nV/$\sqrt{\text{Hz}}$ at the 2 MHz modulation frequency. The accelerometer proof mass was purposely sized to have equivalent mechanical Brownian noise. The noise behavior was measured with a spectrum analyzer under different pressure and modulation voltage as shown in Figure 45. No external forces aside from Brownian noise are driving the accelerometer. The peaks at both sides of the 2 MHz carrier agree with the mechanical resonant frequency of 12.7 kHz. By changing environment pressure and modulation voltage, the noise floor from mechanical limits is verified. The peaks narrow at lower pressure, as expected. The noise floor between 1.98 MHz and 2.02 MHz is primarily mechanical noise with an equivalent value of 45 µg/$\sqrt{\text{Hz}}$ at 760 T at mechanical frequencies below resonance. Predicted and measured data agree. Lowering the modulation voltage, as in Figure 45(b), decreased the transducer gain and reduced Brownian noise seen at the input of the pre-amplifier. High-g accelerometer versions were designed and fabricated, but not yet tested at the time of this report.

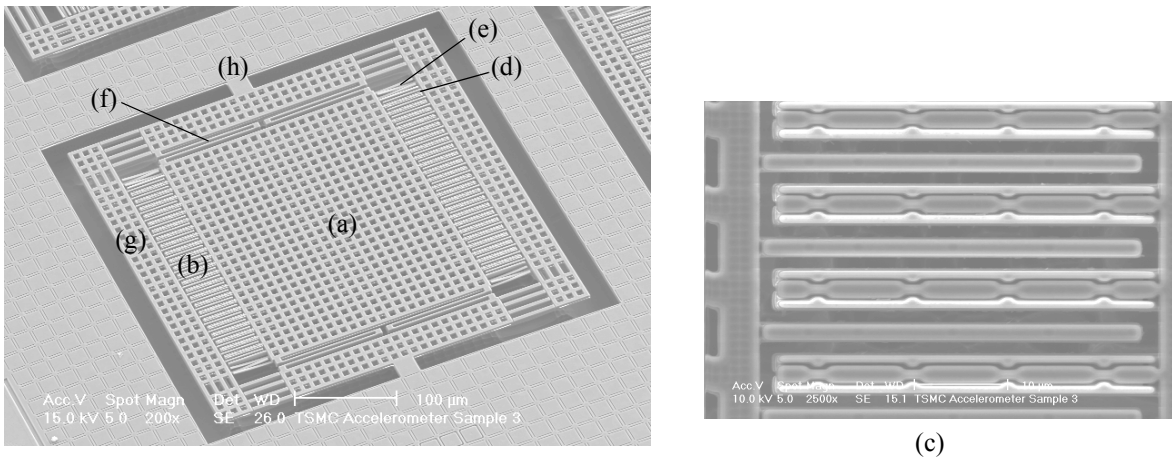


FIGURE 44. Accelerometer in the TSMC 0.35 µm 4-metal CMOS process. (a) Plate mass. (b) Sense fingers. (c) Sense finger close-up. (d) Self-test fingers. (e) Finger limit stops. (f) Spring. (g) Stator curl-matching frame. (h) Anchor.

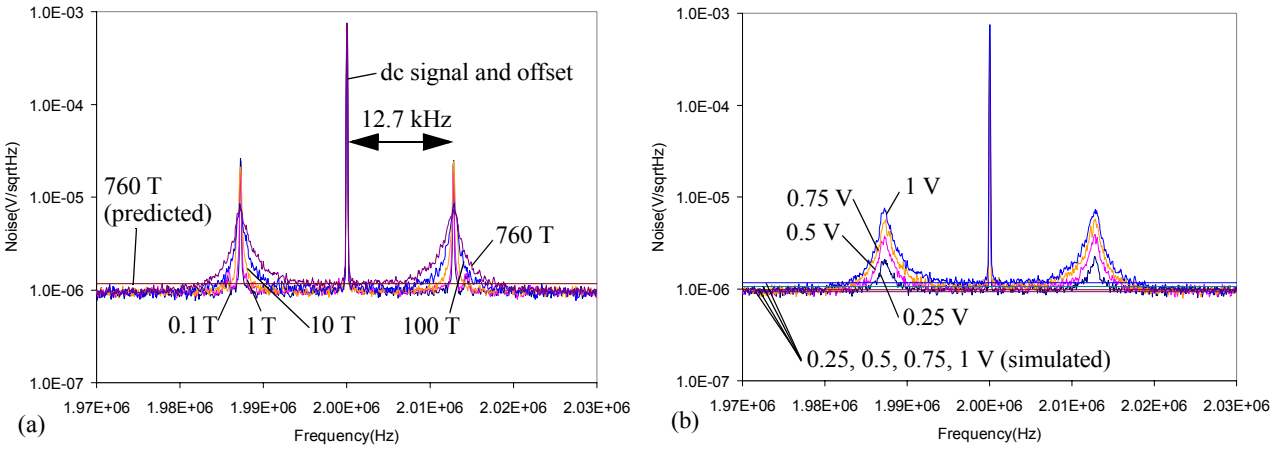
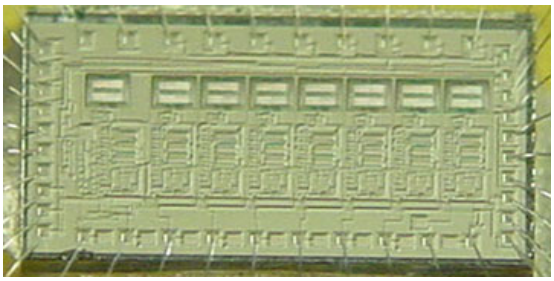


FIGURE 45. Noise measurement (a) with varying pressure and (b) with varying modulation voltage amplitude.

A bulk silicon inertial sensor was developed in conjunction with Bosch researchers [40]. The design was intended to detect acceleration in three-axes. A bulk silicon lateral-axis gyroscope was developed as well [41][42][43][44][45]. The design exploited vertical comb finger sensing and actuation [46][47]. Neither bulk silicon inertial sensor reached brownian noise limits, being limited instead by the interface preamplifier noise.

Inertial sensor arrays. The ASIMPS process allows the integration of arrays of MEMS transducers with electronics. As an example, eight accelerometers were arrayed in development that originally started under the DARPA-MTO-funded "Integrated MEMS Inertial Measurement Unit" project [48]. An image of the chip, and the response of the single and array of accelerometers is shown in Figure 46. The noise of the array was 12 dB higher than a single accelerometer. The signal output from the array was 16 dB higher, leading to an SNR improvement of 4 dB. This was less than the expected 9 dB improvement, implying that the circuit noise dominated the Brownian



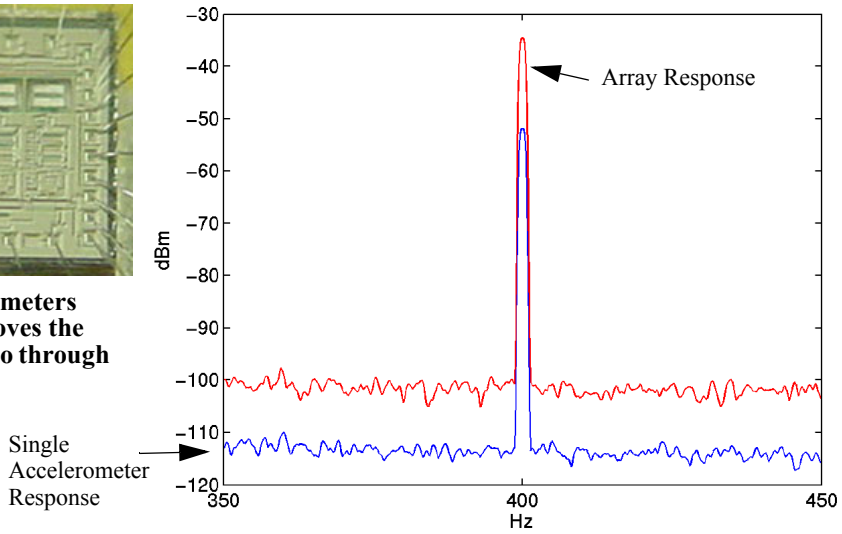


FIGURE 46. Array of 8 accelerometers integrated on a single chip improves the accelerometer signal to noise ratio through averaging.

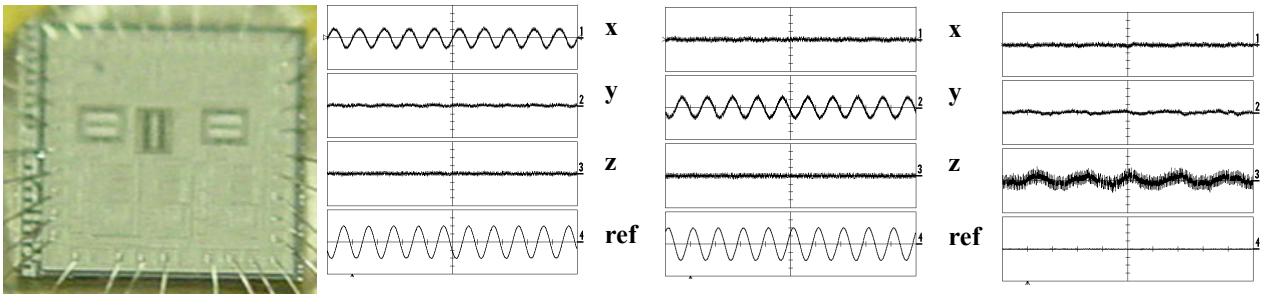


FIGURE 47. 3-DOF IMU (a) chip image; (b) with 1 G acceleration in x-direction; (c) with 1 G acceleration in y-direction; and (d) with manual rotation around the z axis.

noise in this particular design. Another example is the 3-DOF inertial array shown in Figure 47 [49]. The characterization results shown describe the response of the array under acceleration and rotation in the sensitive degrees of freedom. As can be seen in the graph, the lateral x- and y-accelerometer outputs are used to reject against linear acceleration in the gyroscope response.

Bulk Silicon Micromirrors. Single-crystalline silicon (SCS) 1 mm by 1 mm micromirrors were designed in the bulk silicon CMOS MEMS process, with SCS thickness of between 25 µm to 40 µm. The primary application driver was for laser beam scanning in an endoscopic optical coherence tomography (OCT) system. The radius of curvature of the mirror surface from one measurement was 50 cm, much flatter than the thin-film CMOS MEMS due to the stiffening effect of the SCS. The front mirror surface was coated with the top aluminum layer in the CMOS process. A first prototype is shown in Figure 48 [50][51]. The mirror was cantilevered to an elastic hinge structure made with metal 1 and field oxide. The silicon under the hinge was removed by opting to use the timed isotropic silicon etch step in the bulk silicon CMOS MEMS process. The hinge curled up greatly due to the release of high compressive residual stress in the lower field oxide layer along with the low stiffness of the approximately 1 µm structural thickness. For actuation, the hinge was heated by passing current through a polysilicon resistor that meandered within the structure. The temperature coefficient of expansion (TCE) of the top aluminum layer

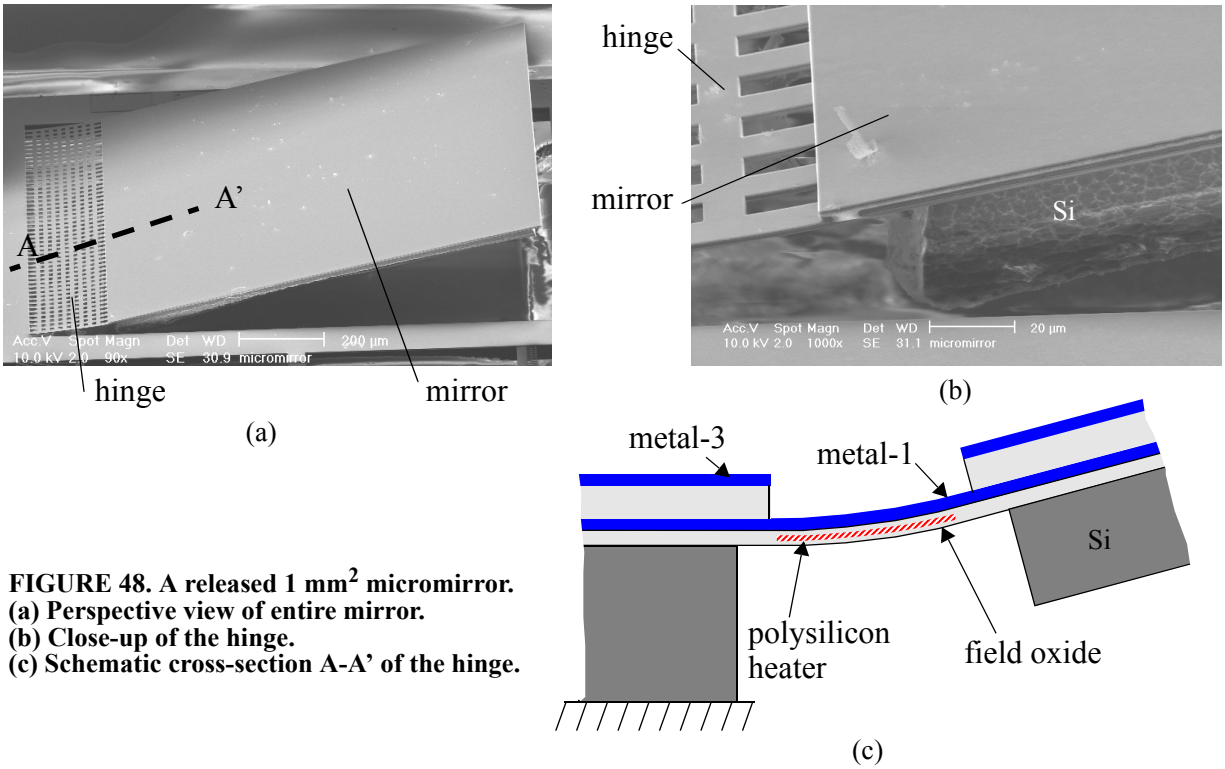


FIGURE 48. A released 1 mm^2 micromirror.
(a) Perspective view of entire mirror.
(b) Close-up of the hinge.
(c) Schematic cross-section A-A' of the hinge.

was greater than that of the bottom field oxide. Therefore, upon heating, the hinge bent down. In the first prototype, the mirror rotated with a range of 30° when 0 to 12 mA current was applied to the 2.4 kΩ heater. The hinge buckled at a critical temperature, creating a step discontinuity between 15° to 20° rotation. After completion of the fabrication, the mirror chip was wire bonded to a small printed circuit board and placed in a 5 mm inner diameter endoscope. The endoscope with the scanning mirror was embedded in an OCT system[52][53][54][55][56]. Cross-sectional images of 500×1000 pixels covering an area of 2.9×2 mm^2 were acquired at 5 frames/s by using the OCT system [52]. Further prototype mirrors, shown in Figure 49, were fabricated and tested. The mirror in Figure 49(a) incorporated a modified beam hinge that eliminated the discontinuity in the rotational response [57]. Mirrors in Figure 49(c) and (d) demonstrated the ability to move in two degrees of freedom using electrothermal actuation [58][59]. These mirrors were tested by Prof. Huikai Xie's group at U. Florida.

CMOS MEMS Acoustic Devices. The ASIMPS project funded seminal work in acoustic CMOS MEMS encompassing devices such as earphones, microphones and ultrasonic sensors. Frequency ranges included audio (20 Hz to 20 kHz) and ultrasonic (up to about 1 MHz), and acoustic media included both air and water.

Chronologically, the first challenge was to find a way to build CMOS-MEMS structures that cover a large area, so that significant volumes of air could be displaced (in the case of actuators) or so that a large compliance was achieved (for microphones in air). Early in the project, a design was found (the "serpentine mesh") that consisted of an arrangement of serpentine springs that could cover a relatively large area [60][61]. This design solved three problems:

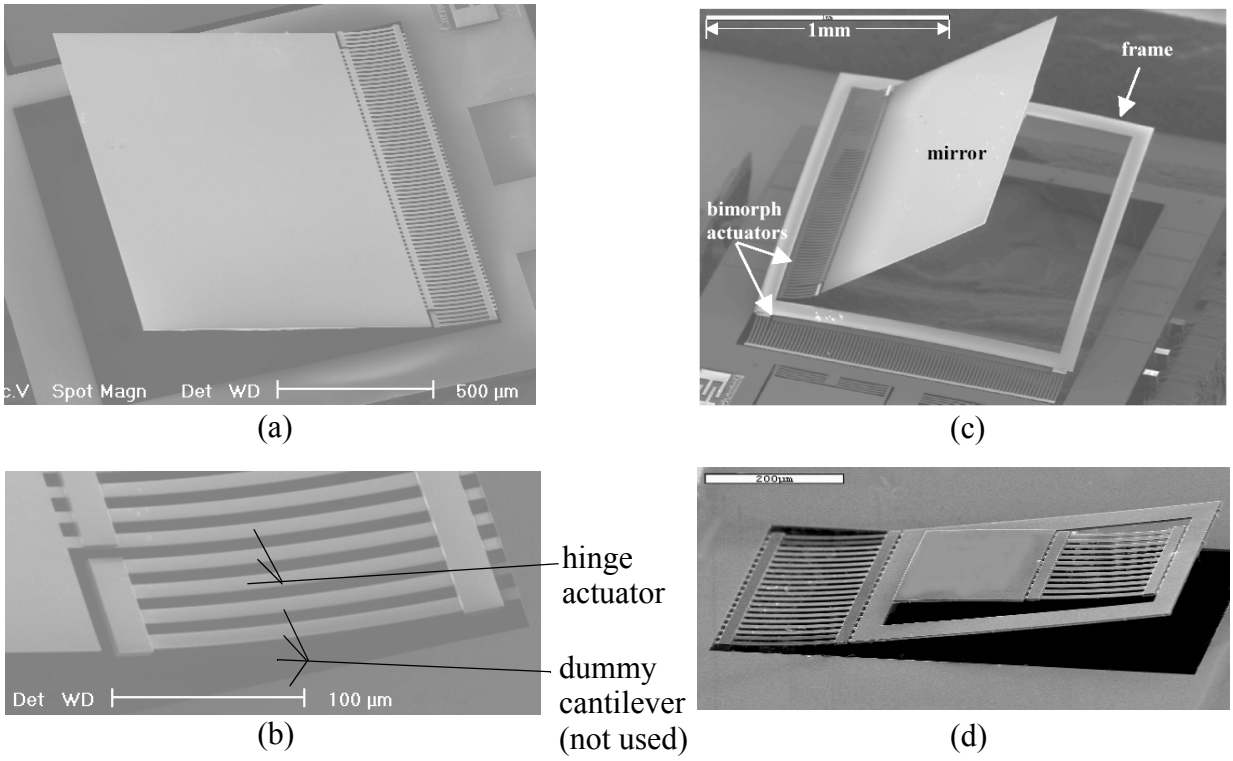


FIGURE 49. Mirror prototypes. (a) Improved single degree-of-freedom 1 mm^2 mirror. (b) Close-up of hinge. (c) Two degree-of-freedom mirror. (d) Piston mirror with two degrees of freedom.

1) The serpentine springs kept individual members short, to minimize out of plane curl.

2) Potential compressive stress was relieved by the springs, avoiding buckling.

3) Gaps were uniform, allowing efficient coating with conformal polymers to create air-tight seals.

This design was first produced on an HP (Agilent) 3-metal 0.5 µm CMOS process followed by post-CMOS micromachining. The initial design submission included one large central membrane 1442 µm on a side, and 27 smaller membranes which encompassed combinations of the beam width, gap size and number of turns in the springs. The meshes were examined optically and with the SEM and it was found that the structures curled out of plane less with smaller unit cells, as expected, due to the shorter maximum beam lengths.

After release of the mesh structure by the post-CMOS micromachining, the chips were actuated and observed optically. With a silicon etch depth of around 50 µm, the 1442 µm square membrane snapped down to the substrate with 65 to 70 V applied between the mesh and substrate. Membranes with smaller etch depths of 10 to 20 µm were fabricated, but the meshes tended to stick to the substrate after voltage was set to zero. This may be due to charging of the oxide layer on top of the silicon substrate or from membrane buckling.

Several methods were investigated to coat the meshes to make them airtight. The approach leading to the best results for the acoustic applications was a conformal polymer deposition in a plasma of C_4F_8 in an STS (Surface Technology Systems) deep silicon etcher. The C_4F_8 is nor-

mally used in the Bosch deep silicon reactive-ion etch process as a sidewall passivation cycle. Another technique attempted for mesh sealing was spinning polymer (Pyralin 2555) onto the chip, but viscosity of the polymer solution ripped the membrane off the chip. A modification involved spinning polymer onto a wafer, placing the membrane chips face down into the polymer, and peeling off the polymer after curing. This also did not give acceptable results as the polymer did not make consistent contact with the membranes, which are a micron or two below the chip surface. Another unsuccessful method was vapor coating with parylene C (performed by Specialty Coating Systems, and Para Tech). The parylene should have conformally coated the chip as the monomer, vaporized in a low pressure environment, adhered to the chip surface and crosslinked to form the polymer. However, when these chips came back for testing, the membranes could not be actuated. The reason for this is still unknown, but two possibilities are:

1) The parylene is thicker or stiffer than originally anticipated. According to Advanced Coating Systems, the minimum thickness is around 0.1 mils = 2.54 μm.
2) The polymer went through gaps in the mesh and made a mechanical connection to substrate, fixing the membrane in place.

Polymer Quality. The polymer that was put down by the C_4F_8 plasma in the STS machine varied in quality, from being soft to flaking off when scratched with a microprobe. Chemical tests were not performed, however the difference in properties was possibly due to variations in process chamber conditions between runs causing differences in cross-linking and/or stoichiometry. Cracking was also observed, usually following a straight line along boundaries of the unit cells in the mesh.

In 2004, a spin-on polymer (specifically, polystyrene dissolved in toluene) achieved a uniform coating that clings to the serpentine mesh structure without collapsing it or ripping it off the chip during spinning. In order to see the extent of the polymer sticking to the mesh, and whether it dripped through or caused collapse, a probe tip was used to puncture and tear the membrane and lift it so the torn edge could be viewed head on. The coated mesh is shown in Figure 50.

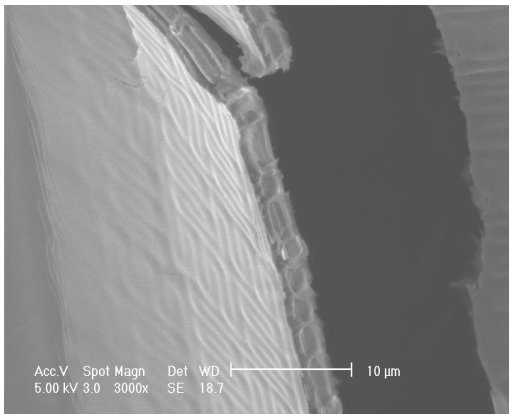


FIGURE 50. Mesh coated by spin coating a layer of polystyrene dissolved in toluene.

Through-Wafer Vent Holes. Vent holes connecting the sub-membrane gap to the back side of the chip were necessary for audio frequency acoustic applications. For this purpose, silicon DRIE was used to etch through the chip. Several design approaches were used, with their own advantages and disadvantages.

In the first approach, holes were patterned on the back of the chip with photoresist and a deep etch was made until the CMOS layers (i.e. the oxide layer below the metal) was reached. Then the chips were etched from the CMOS (top) side to release the structures. The advantage of this

method is its simplicity, especially the timing of the deep etch from the back could be slightly longer than the time needed to reach the oxide, due to the selectivity of the etch to silicon over oxide. There were two disadvantages though. First, the removal of silicon from underneath the structures left behind a fragile glass "window" which could easily be broken in handling, for example when removing the chip from the carrier wafer used in the etch. Later this was solved with photoresist stripper soak, which gently removed the photoresist attaching the chip to the carrier. Another issue is that the slight etching of the backside of the oxide layer caused uneven stresses in the membranes over the vent holes, resulting in dimples.

A second approach was to perform the backside etch, but time it so the etch stopped about 5 μm before the oxide. Then, the chips were processed from the front in the usual way, and the silicon underetch also opened up the vent holes. This resulted in good quality membranes, though the backside etch process needed close attention to etch rate, and several optical depth measurements during the etch.

A third approach was used for the digital speaker arrays, where membranes were smaller and tolerances were tighter for placement of vent holes [62][63]. A large rectangular area was etched from the back, encompassing the area of all the membranes, and reaching within a few microns of the CMOS surface. Then a vent hole pattern was aligned on the front side (to the membranes). The vent hole etch was performed from the front, photoresist was removed, and then an unmasked etch was performed to release the membranes.

In all approaches above, the photolithography was complicated by the difficulty in applying photoresist coatings to small chips (as opposed to wafers). The size of the edge bead or edge effect region is often comparable to the size of the chip. This was mitigated by spinning several thinner layers of resist, or in some cases by putting "dummy" chips around the chip being coated in order to reduce edge effects.

Acoustic Model Development. Lumped parameter acoustic models were developed in order to predict performance and aid in design. These models also yielded insight into the acoustic physics such that general statements could be made about the suitability of (CMOS) MEMS devices for different applications. For audio frequencies, the relevant wavelengths were always significantly larger than the MEMS devices, so a lumped parameter electrical equivalent model was always appropriate. Standard acoustic textbook models were found to be relevant at the MEMS scale, except in the case where heat transfer was taken into account between the silicon substrate and compressed/expanded air in the sub-membrane gap (a compliance expression based on an isothermal compression was found to be more appropriate than the adiabatic compression equation usually used in acoustics).

Based on familiarity with the acoustic models, several (theoretical) statements hold:

1) MEMS microphones should have superior vibration insensitivity compared to conventional microphones. This is due to the smaller areal density of the diaphragms.
2) For a given total working area (subdivided into appropriately sized diaphragms) the thermomechanical noise should be less for diaphragms with small areal density.
3) Using MEMS speakers for transmitting sound in air is nearly hopeless at audio frequencies, because of the tiny radiation impedance (due to the small area). However, a modestly loud

(70-80 dB SPL in the ear canal) earphone was demonstrated due to the nearly sealed environment of the ear. Another near exception would be ultrasonic transmission in air, as the radiation impedance increases rapidly with frequency at small size scales. Transmission/ echo detection have been demonstrated by ETH Zürich over distances of several cm.

4) Diaphragms vibrating in the lowest order mode may be the simplest way for a MEMS device to perform gravimetric detection in fluid. Though the diaphragm experiences heavy mass loading (10 to 100 times the diaphragm mass), the radiation loss (the primary damping mechanism) is modest at lower frequencies.

Speakers. The first acoustic device demonstrated in the ASIMPS process was an earphone [60][61]. This incorporated the 1442 µm square membrane chip. As mentioned earlier, this depended on the etching of vent holes, in addition to the usual CMOS-MEMS micromachining, to achieve a usable acoustic system. In addition to the chip processing, overall packaging was important to the function. The front side of the membrane had to face into the ear canal, and the back side had to be vented into an air volume large enough to present an acoustic impedance comparable to or smaller than the membrane. Furthermore, the housing also had to create a tight seal to the ear canal to avoid an acoustic short circuit to "ground" (ambient pressure). For the housing, we used the plastic shell of an inexpensive commercially available earphone.

Speaklet Arrays. While individual speaker membranes have an unimpressive linearity and range of motion, it is possible to improve on this by exploiting the ability of MEMS to create many copies of a simple structure (multiplicity). A chip with an array of 255 "speaklets", each 216 µm on a side, was electrically grouped into binary sets of 1,2,4...up to 128 so they could be directly driven with a binary word [62][63]. To a crude approximation (ignoring the effects of varying distance to different parts of the array) the pressures from the individual speaklets add together, resulting in a sound pressure that is proportional to the input binary word. This "Digital Sound Reconstruction" concept was demonstrated by the bit-by-bit reconstruction of a sine wave, shown in Figure 51. The frequency response of the device is shown in Figure 52 while driving all the speaklets with an analog voltage vs. driving the array with the corresponding digital word stream. While the speaker array shows a great improvement in sound volume over the earphone, and potential for superior linearity and frequency response, CD-quality sound requires at least 16 bits (>65,000 speaklets), and the audio industry is moving toward 24 bits. However, 8 bits is sufficient for intelligible speech.

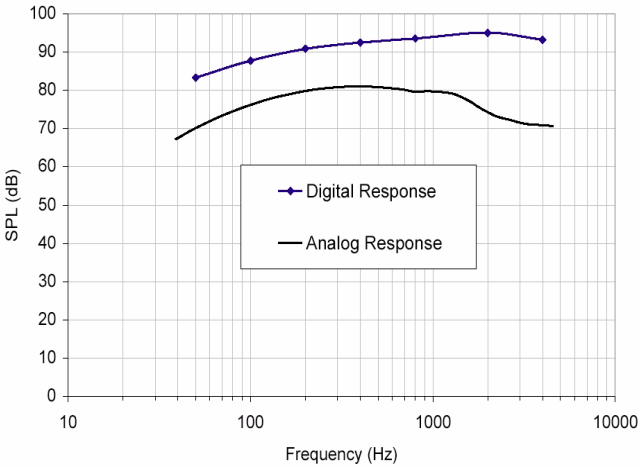


FIGURE 51. Output level from speaker array when driven by digital words, and with an analog voltage.

Microphones. Two generations of microphones were fabricated, using CMOS membranes as sensing elements [64][65][66]. In these designs, the deflection of the membranes was sensed by

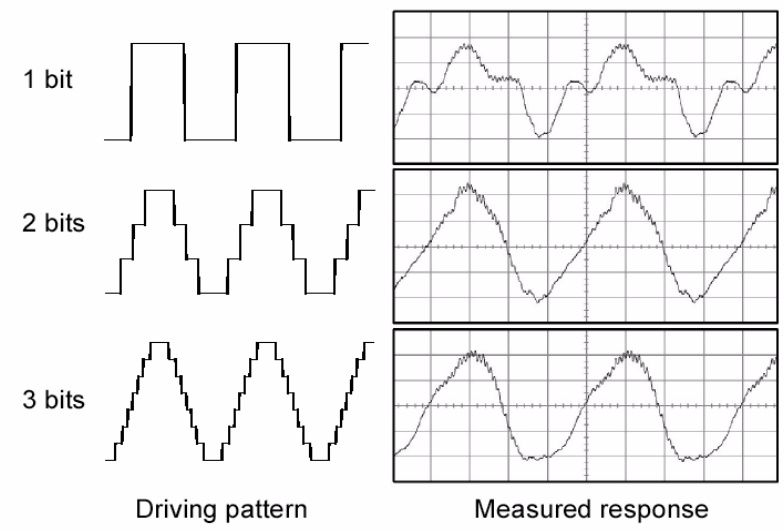


FIGURE 52. Bit-by-bit reconstruction of a 500 Hz sine wave.

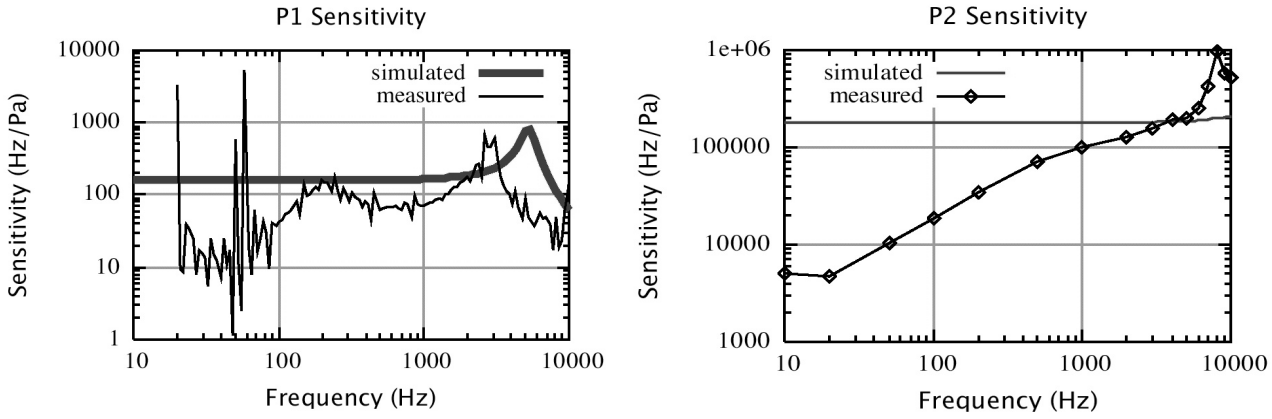


FIGURE 53. Responses of the two generations of microphone prototypes, P1 and P2.

measuring the capacitance between the membrane and substrate. Because one side of the capacitor is always the substrate, connected to the negative supply voltage, the range of circuit topologies for measuring the capacitance is severely limited. To demonstrate the proof of concept, and to compare sensitivity response to theory, it was sufficient to incorporate the membrane-substrate capacitance into an oscillator and measure the frequency shift for a given sound pressure. The frequency shift was predicted from acoustic considerations, the size of the gap, and extraction of the parasitic capacitance from the chip layout.

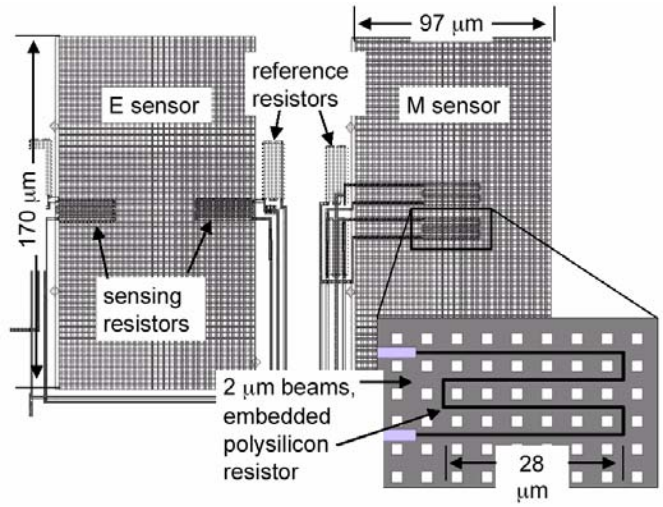


FIGURE 54. Layout of ultrasonic sensor diaphragms, showing dimensions and placement of piezoresistors.

Ultrasonics. Efficient generation of ultrasonic waves using the CMOS MEMS membranes, in either air or water, has not yet been demonstrated. However, membranes were designed in a range of acoustic impedances that are near and below that of water, and so make excellent receivers [67]. The low acoustic impedance of the CMOS MEMS membranes means they closely track the fluid motion, which leads to a wide frequency response. With CMOS MEMS membranes, it is also straightforward to incorporate a piezoresistor in the membrane to sense deflection, which allows fabrication of sensor elements much smaller than capacitive sensors of comparable sensitivity.

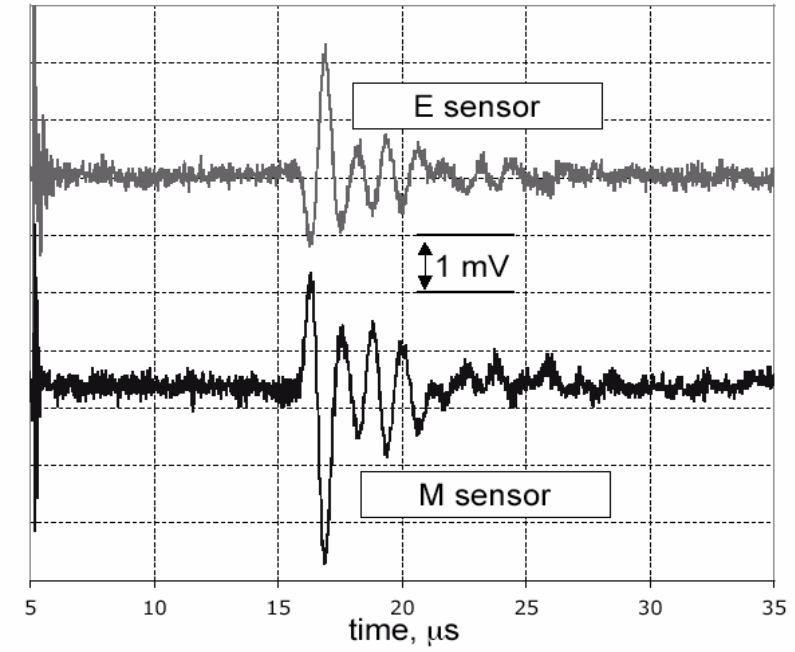


FIGURE 55. Measured waveforms from E and M placements of piezoresistors. A potential of 10 V was placed across opposite corners of the resistor bridge, and the differential signal is shown. The peak displacement of the diaphragm center, estimated from other measurements, is approximately 7 nm.

Collapse of large membranes. In instances where the membranes were large, or when gaps were very small, the membranes stuck to the substrate either after actuation or immediately after processing. In some cases, the membrane after a long time (order of days) would pull back up. This effect is believed to be a competition between the elastic force pulling the membrane up vs. a residual electrostatic force, due to charging of the oxide layer, pulling the membrane to the substrate. In the cases of membranes pulling back up after long periods of time, this is explained by a gradual discharge of the oxide.

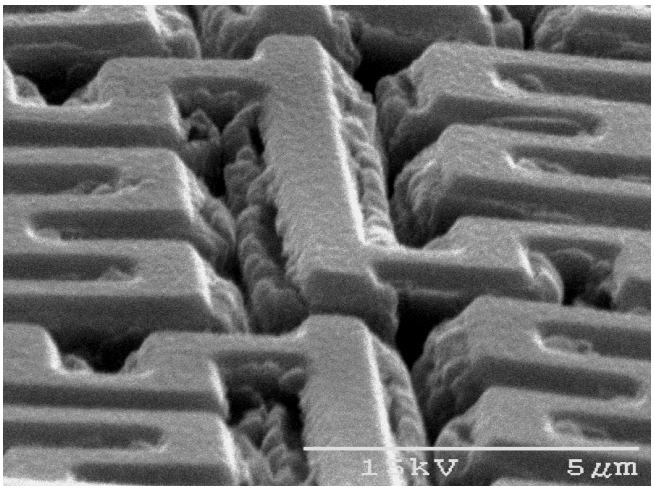


FIGURE 56. CMOS mesh after treatment with pad etch vapor. It appears that reaction products are not removed without immersion in liquid.

Oxide removal. In an attempt to achieve small gaps, and eliminate bimorph stress curling, an attempt was made to remove oxide from underneath the metal layers. The first method exposed the chip to a vapor of HF. This appeared to remove oxide, but it also degraded the aluminum surface. Another second chemical vapor treatment was tried, "Pad Etch III", (Advanced Chemical Systems International Inc., 50% acetic acid, 20% ammonium fluoride) which did something to the oxide, in that it appeared to get thicker and irregular in appearance, but the treatment did not remove it. Vapor rather than direct immersion in liquid was used to avoid surface tension stiction.

Effective Young's modulus of the polymer membranes. The Young's modulus of the polymer, which is assumed to dominate the stiffness of serpentine mesh type membranes, was measured indirectly by two methods. In one method, the voltage on a membrane was gradually increased until snap-down occurred. The effective Young's modulus was extracted from the membrane geometry and an analytic formula, and calculated to be between 100 MPa and 10 GPa, not nearly accurate enough for design use. In the other method, both the Young's modulus and the density were extracted from comparison of acoustic measurements with acoustic models and found to be between 800 MPa and 1 GPa. In the first case, the very wide uncertainty comes in part from the varying amount of polymer relative to metal and oxide structure. Interestingly, in some of those measurements, as the gaps in the mesh are sealed, the effective Young's modulus rises rapidly from 200 MPa to about 1 GPa. This is evidence that the polymer stiffness dominates over the underlying mesh structure. Some of the other inconsistencies arise from neglect of non-linear effects in the snap-down experiment, and perhaps also because of cracking or fatigue of the polymer in the snap-down experiment. In the acoustic experiments, there appears to be a range of values because the density is also uncertain. Improvements to both of these procedures would be obtained by making a correction for the inherent stiffness of the mesh structure.

Acoustic Leaks. As mentioned earlier, performance of acoustic MEMS depends as much on packaging of the device as the on-chip structures. Particularly important for the microphones is the isolation of the front and back of the diaphragm. Devices with a resistive path connecting the front and back caused a low frequency roll-off (high-pass filter). It was observed to some extent in both generations of microphone prototypes fabricated, especially the second one. Experimental attempts to find the leak failed, but it should be noted that others (Akustica, Inc.) have found that changing the type of glue on the package can have an unexpectedly large effect (even when the glue appears to be sealed well).

Gravimetric biosensing. The CMOS membrane technology is currently being applied to gravimetric biosensing, the goal being to construct a diaphragm that will change resonant frequency

when a target chemical species is adsorbed. The main difficulty of this application is to isolate the driving and sensing modes within the same device. In the first prototype, which used capacitive sensing, application of a drive voltage caused an overloading of the high-impedance amplifier, with a long recovery time (the drive and sense were independently tested, and worked as expected). In the second prototype, piezoresistors were used as the sensing mode, but the polysilicon resistors were sensitive to the *transverse* electric field from the drive. A subsequent search of the literature confirmed that this effect had been seen by others. At the ASIMPS project conclusion, a third prototype was being planned, which would use piezoresistors with additional shielding to protect them from the drive voltage electric field.

5. Conclusions

The prime objective to build ASIMPS into a self-supporting service by the end of the project was met, albeit along a path none of the investigators could imagine. The acquisition of the JDS Uniphase MEMS unit by MEMSCAP paved the way for the commercialization of the process service. By the second year of the project, it was clear that use of wafer-level processing to implement a prototyping service was not optimal. The cost of engineering runs for the wafers was far more expensive than what users would pay. The chip level processing was viable for prototyping once a foundry was identified that would support both chip-level multi-user project runs and also support wafer level runs in the event a user wished to ramp up to production. The teaming of MEMSCAP with Jazz Semiconductor provided the opportunity, as Jazz was willing to provide CMOS chips in their BiCMOS process for ASIMPS. The 0.35 μm process is superior to cruder CMOS, having better stress matching between the metal and dielectric layers. The resulting microstructures were very flat and provide general microsystem design capabilities that exceed those currently offered in non-integrated MEMS foundry processes.

The design tools also advanced in this project, particularly with the capability to build CMOS MEMS schematics in 3D within the Cadence design environment. The MEMS element models are available for customization to other design environments as well.

Specific advances were made in design of CMOS MEMS accelerometers. The low g accelerometers were verified to achieve brownian noise limited performance that rivals that of polysilicon accelerometers made in captive foundry MEMS processes. High g accelerometers were designed and fabricated. These devices have yet to be tested, but signify a step toward high performance integrated high-g arrays for DoD use. The micromirror development has spawned interest from groups interested in single mirrors and large area mirror arrays for laser scanning applications. The ASIMPS development has enabled a entirely separate design thrust in RF MEMS with high-frequency electronics to create low noise, low power voltage controlled oscillators, bandpass filters and down-converting mixers on chip for eventual cognitive transceivers. The CMOS MEMS membrane process has enabled commercialization of microphones with digital signal processing and microphone arrays for cell phones and other consumer applications. It maybe reasonably expected that more applications and commercial impact will result from the expected wider offering of ASIMPS in the coming years. This potential for new integrated microsystems was enabled by the DARPA ASIMPS funding.

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7. List of Symbols, Abbreviations, and Acronyms

AHDL - Analog Hardware Description Language
AMS - Austria Mikro Systeme
ASIMPS - Applications Specific Integrated MEMS Process Service
BiCMOS - Bipolar / CMOS [transistor process]
BEA - Boundary Element Analysis
CAD - Computer Aided Design
CMOS - Complementary Metal Oxide Semiconductor
CMP - Chem-Mechanical Polishing
CPU - Central Processing Unit
DARPA - Defense Advanced Research Projects Agency
DoD - Department of Defense
DOF - Degree of Freedom
DRC - Design Rule Check
DRIE - Deep Reactive Ion Etching
ETH Zürich - Eidgenössische Technische Hochschule
(Swiss Federal Institute of Technology) Zürich
FEA - Finite Element Analysis
FIB - Focused Ion Beam
FIBE - Focused Ion Beam Etching
HF - Hydrofluoric Acid
HP - Hewlett Packard
IMIMU - Integrated MEMS Inertial Measurement Unit project
MEMS - Micro Electro Mechanical Systems
MIT - Massachusetts Institute of Technology
MOSIS - Metal Oxide Semiconductor Implementation Service
OCT - Optical Coherence Tomography
RF - Radio Frequency
RIE - Reactive Ion Etching
SCS - Single Crystal Silicon
SPL - Sound Pressure Level
STS - Surface Technology Systems
TCE - Temperature Coefficient of Expansion
TSMC - Taiwan Semiconductor Manufacturing Corporation